

100_Power On Timing--AC mode
101_Power On Timing--DC mode

Docking(GC31/GC32/GC32_refresh)



PCIE/WLAN/LAN/SSD

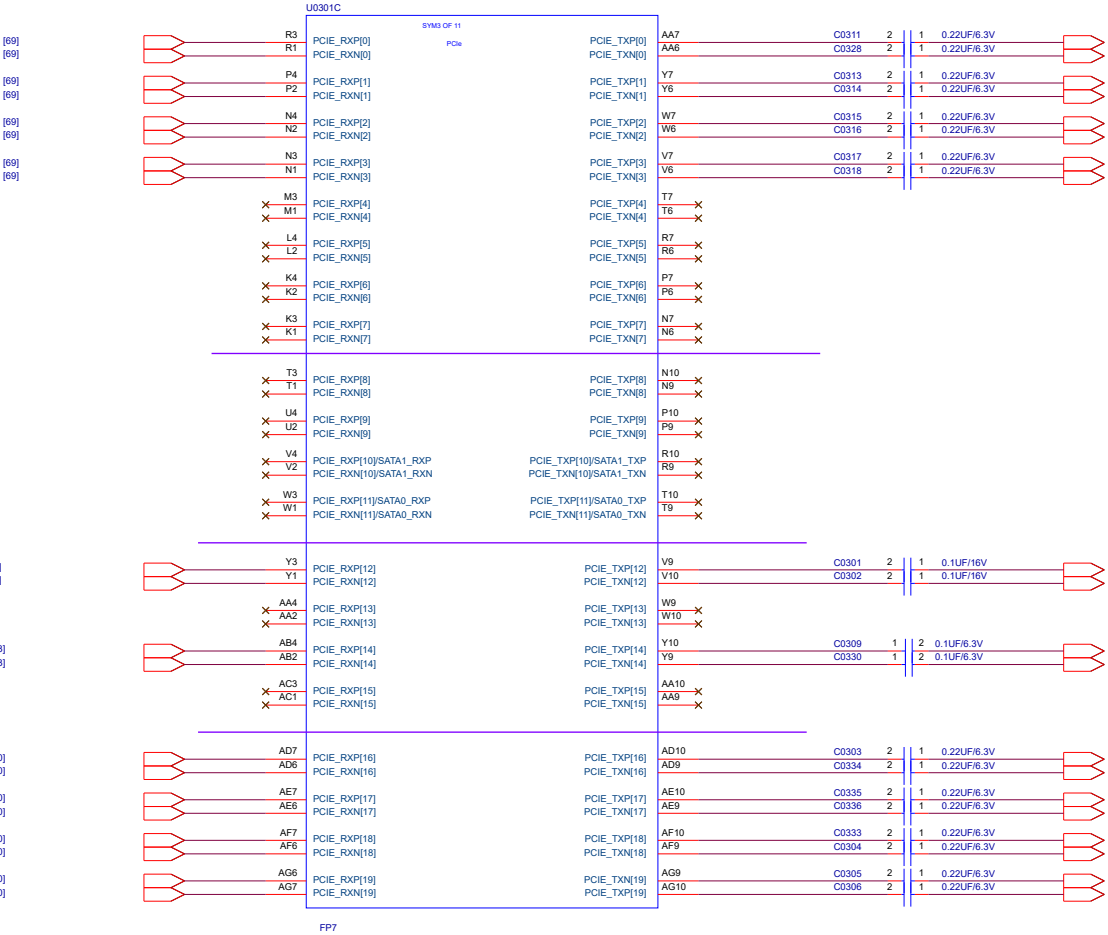
RX Side

PCIE NB RX [0~7]

PCIe x1	CR1	lane 4	[42]
PCIe x1			[42]
PCIe x1	5G	lane 6	[53]
PCIe x1	WLAN	lane 7	[53]
		lane 0	[40]
		lane 1	[40]
PCIe x4	SSD	lane 2	[40]
		lane 3	[40]

CPU TX to GPU RX (Onboard device)
CPU RX to GPU TX
CPU TX to M.2 TX (CON.)
CPU RX to M.2 RX
CPU TX to WLAN TX (CON.)
CPU RX to WLAN RX
CPU TX to LAN RX (Onboard device)
CPU RX to LAN TX

20191029, cap. selection related to PCIE speed
Gen3: with 220nF
Gen2: with 100nF



TX Side

PCIE G TX [0~7]

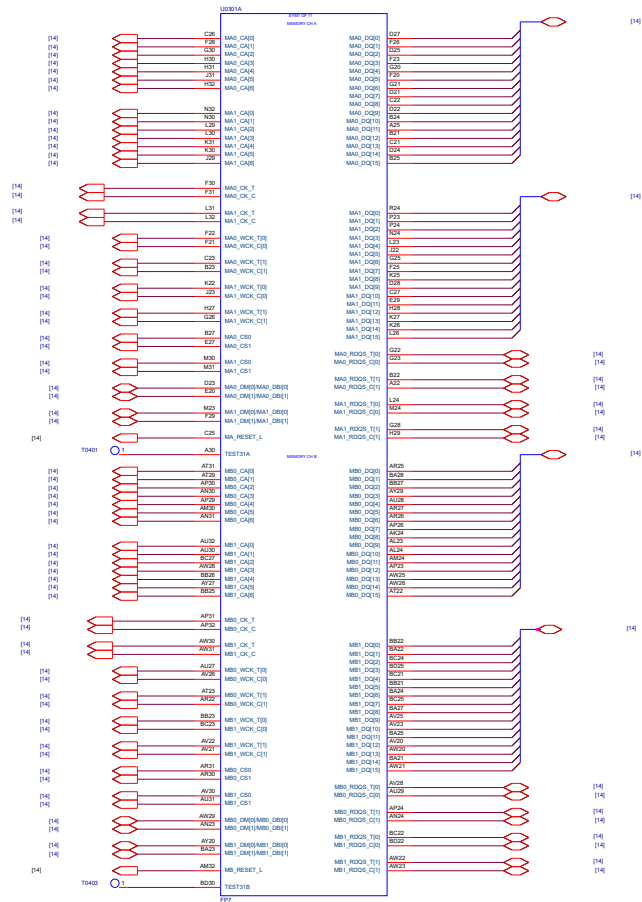
lane 4	[42]
lane 5	[42]
lane 6	[53]
lane 7	[53]
lane 0	[40]
lane 1	[40]
lane 2	[40]
lane 3	[40]

ASUS		Project Name	Rev
		GV301	R1.0
Title : AMD_CPU_PCIE			
Size	Dept.: ASUSTeK COMPUTER INC Engineer: NR EE RD3		
B			
Date: Wednesday, January 18, 2023		Sheet	3 of 104

Memory Channel A/B

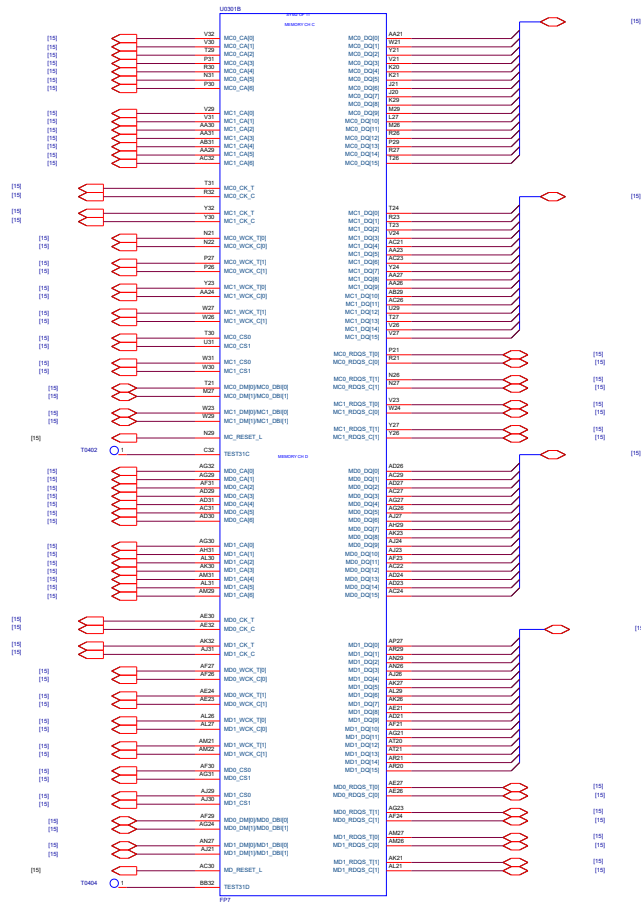
20210305 LPDDR5 DRAM down/pin swap follow MAYAN CRB

On Board LPDDR5



Memory Channel C/D

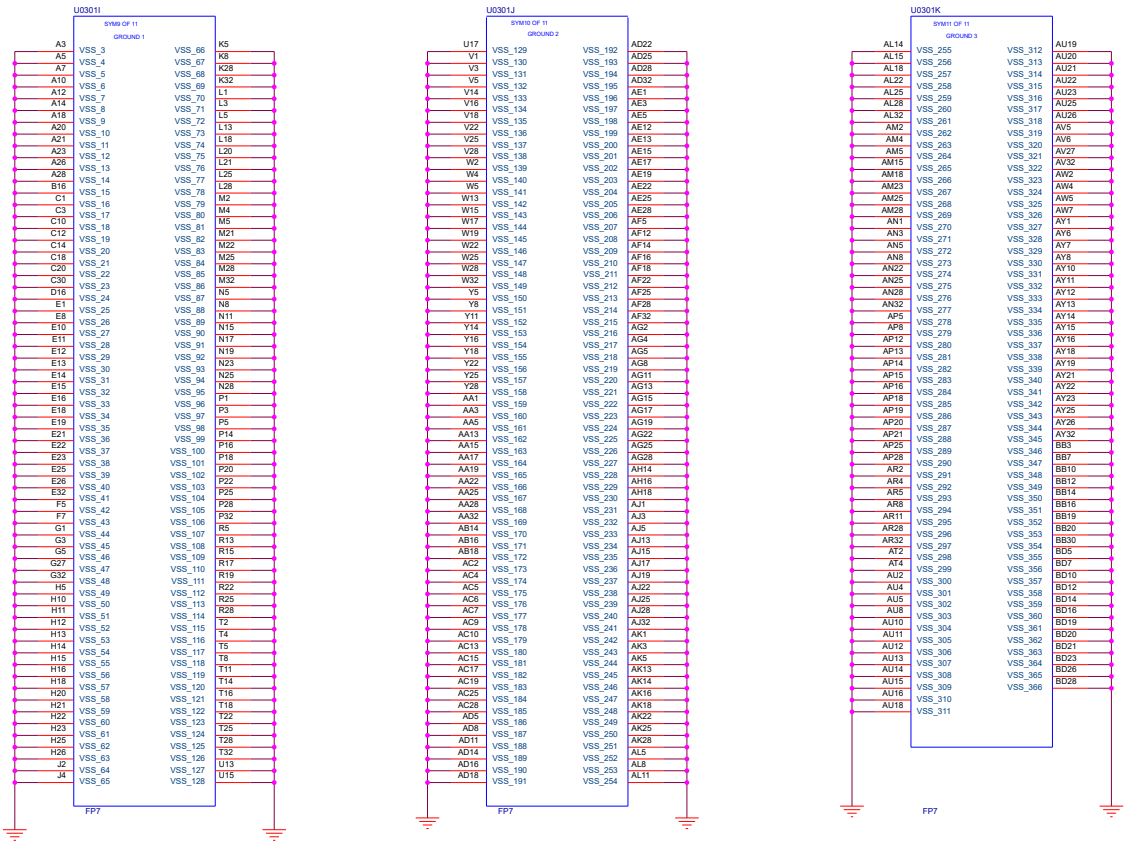
On Board LPDDR5



Main Board

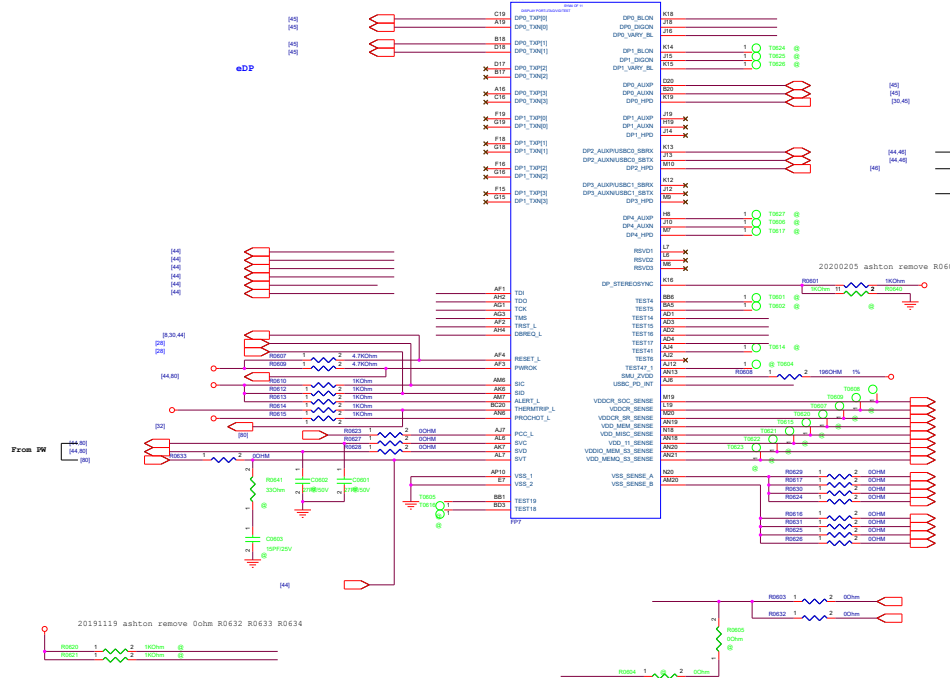
		Project Name GV301	Rev R1.0
Title : AMD_CPU_DDR4			
Size C	Dept.: ASUSTeK COMPUTER INC.		Engineer: NR EE RD3
Date: Wednesday, January 18, 2023		Sheet 4 of 104	

CPU_GND

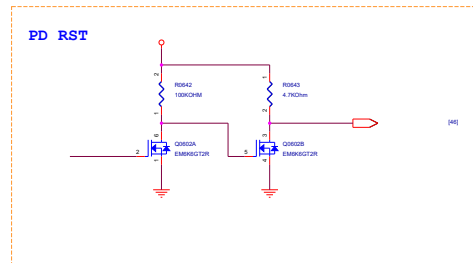


Display

Display Port TX/RX
O-IOVP-D_VDDP (S0_0.75)_FP6 (FDS)



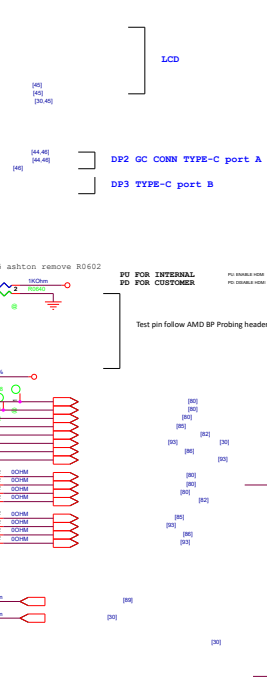
PD RST



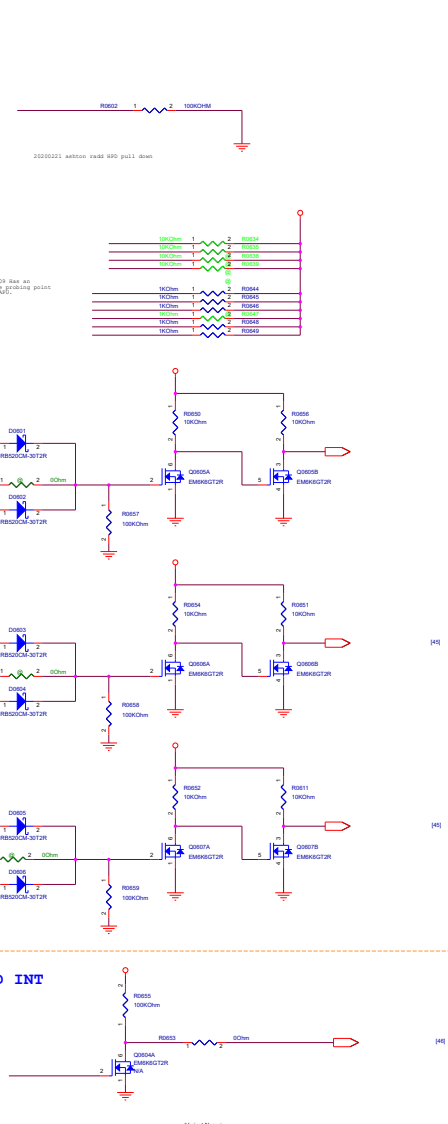
與POWER討論此PIN改由SW動作拉降頻(cost down)
故此PIN不接
P.30 & P.78 DGPU_LIMIT
@20181015E

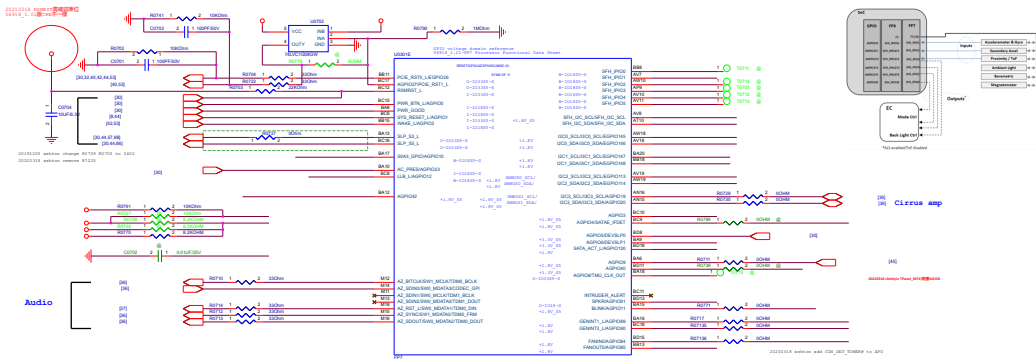
20200205 ashton removeC0602,C0604,C0605,C0606

Display Panel
O-IO18-S (S0_1.8)_FP6 (FDS)



Display Port HPD
I-IO33-S (S0_3.3)_FP6 (FDS)

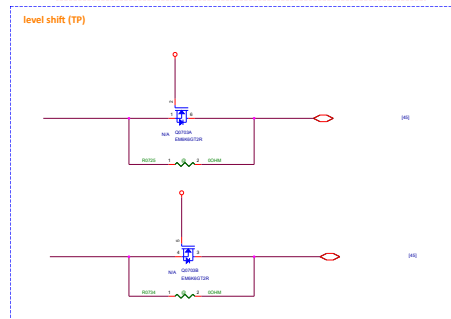
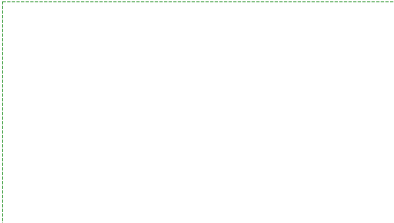
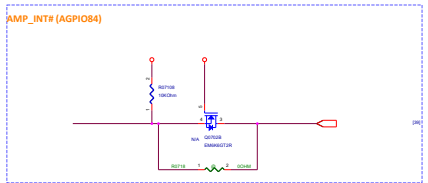
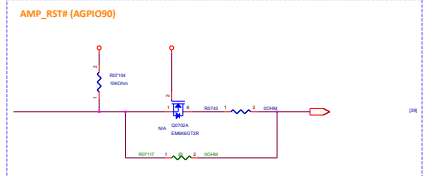
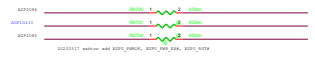
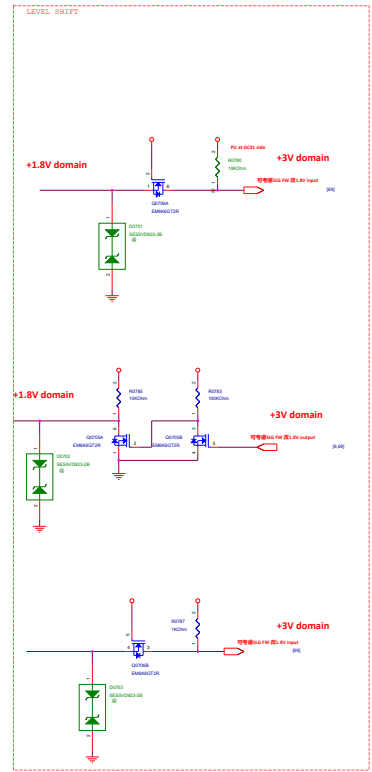




Clears amp

Card Reader

20200515 adden add C2D_VT1_1000000 to BJT



20200515 change Memory strap, DIMM_SEL2 change AGP085

Onboard Memory PCB-ID:
AGP084 =>02DMM_SEL2
AGP085 =>02DMM_SEL2

LPDDR5 Memory Down pool

以下為目前 on-board SDRAM strap pin definition(host side, Gaming BU), FYI.

ASUS P/N	Company	Vendor P/N	[MT/S]	Total Size/Chip	DIMM_SEL2 Intel(GPP_A8) AMD(AGP085)	DIMM_SEL1 Intel(GPP_E16) AMD(AGP04)	DIMM_SEL0 Intel(GPP_E0) AMD(AGP06)
LPDDR5							
03015-00070000	Micron	MT62F1G32D4DR-031 WT-B	6400	1024x32 (32Gb)	L	L	L
03015-00070200	Samsung	K3LKB8B0BM-MGCP	6400	1024x32 (32Gb)	L	L	H
03015-00080000	Micron	MT62F2G32D8DR-031 WT-B	6400	2048x32 (64Gb)	L	H	L
03015-00080200	Samsung	K3LCKC0BM-MGCP	6400	2048x32 (64Gb)	L	H	H
DDR5							
03016-00050000	Micron	MT60B1G16HC-48B-A	4800	1024x16 (16Gb)	H	H	H
03016-00010000	Samsung	K4RAH160VB-BCKR	4800	1024x16 (16Gb)	H	H	L
03016-00010100	SKhynix	H5CG16MRDAX	4800	2048x16 (16Gb)	H	L	L

CPU CLK

@20190624A

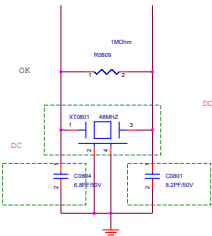
CLKREQ6_GPU# --> CLKREQ0_GPU#

CLKREQ0_SSD1# --> CLKREQ4_SSD1#

CLKREQ3_SSD2# --> CLKREQ5_SSD2#

CLKREQ1_WLAN# --> CLKREQ6_WLAN#

PCIe CLK B/N
後端記得預留 0 ohm



GPU

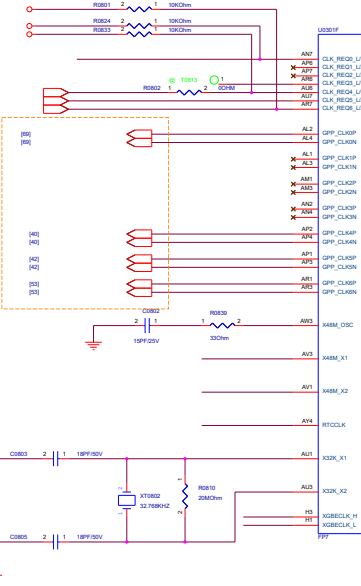
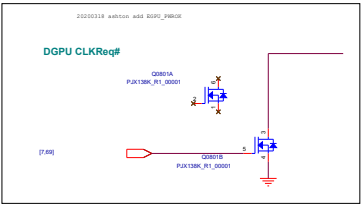
5G

CR2

SSD2

CR

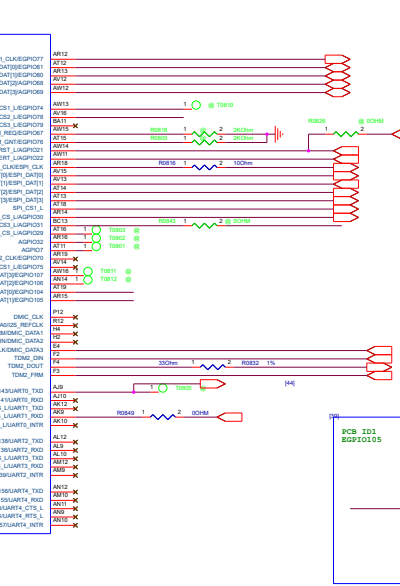
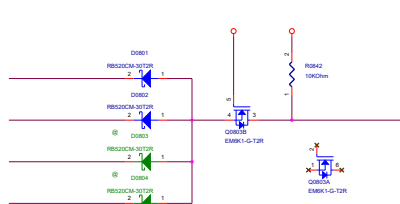
WLAN



SPD voltage domain reference
S601_1-12-1977 Programmer Functional Data Sheet

SPD voltage domain reference
S601_1-12-1977 Programmer Functional Data Sheet

SPD voltage domain reference
S601_1-12-1977 Programmer Functional Data Sheet



eSPI

SPI

SPI

SPI

SPI

SPI

SPI

SPI

SPI

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SPI

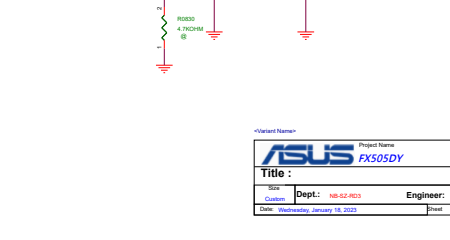
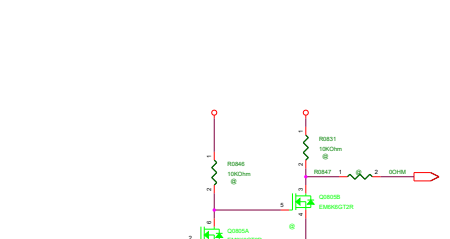
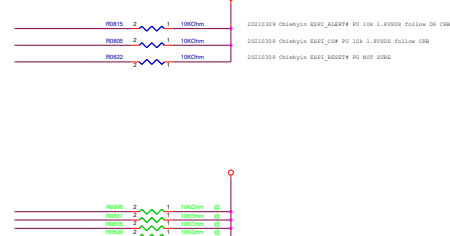
SPI

SPI

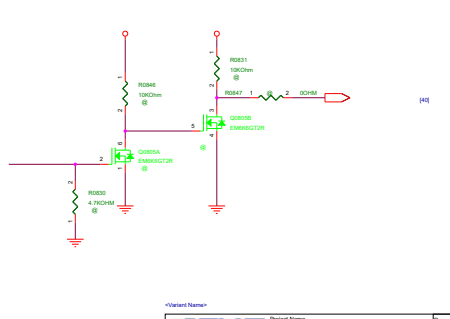
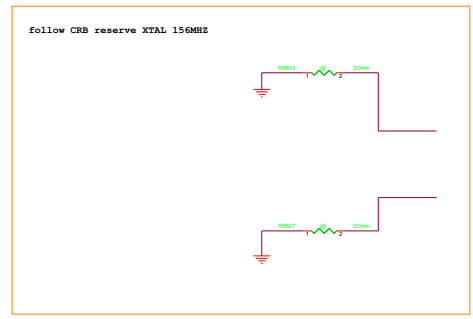
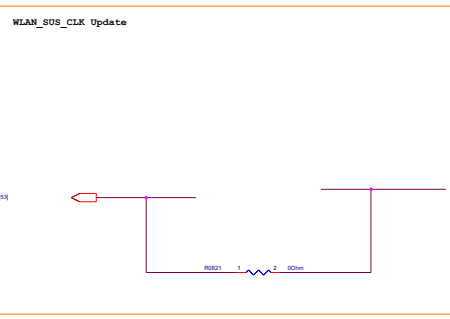
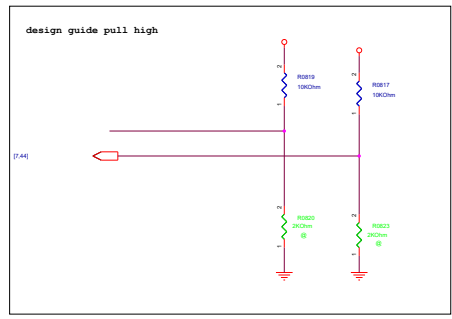
SPI

SPI

SPI

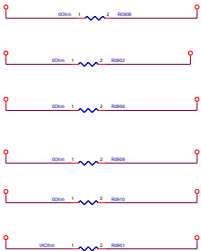


20191119 ashton remove S10805 S10802

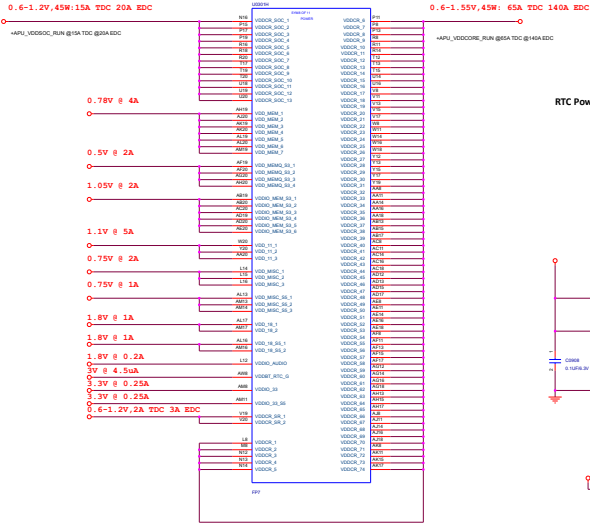


Project Name		Rev
Title		R1.0
Customer	Dept.: NB-G2-R03	Engineer:
Date: Wednesday, January 10, 2024	Draw: 6	of 104

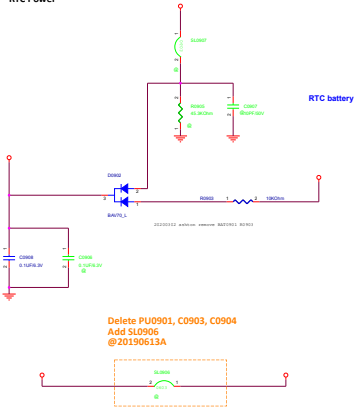
CPU_Power



11G232210526360 (11UF/10V) change to 11G232210515320 (11UF/6.3V)
C0902
@20190705C

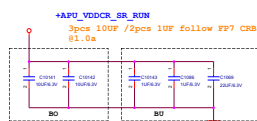
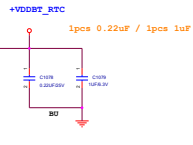
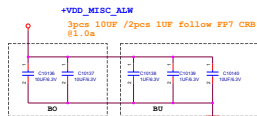
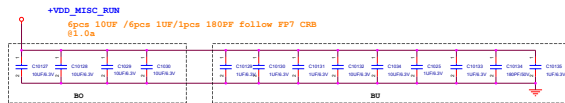
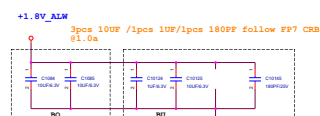
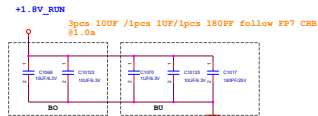
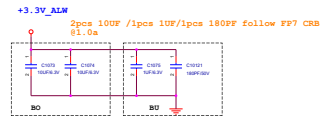
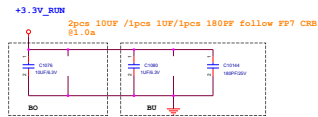
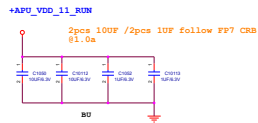
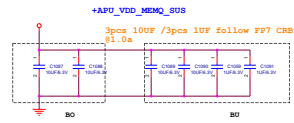
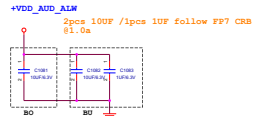
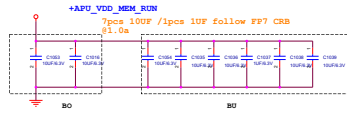


RTC Power



CPU_CAP

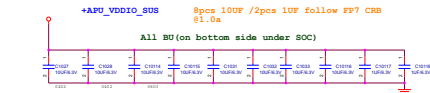
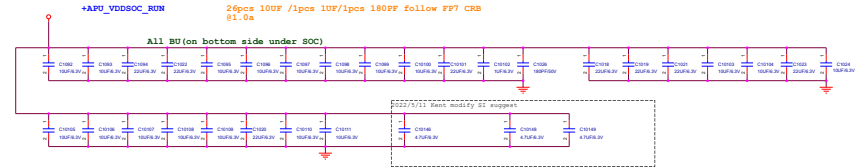
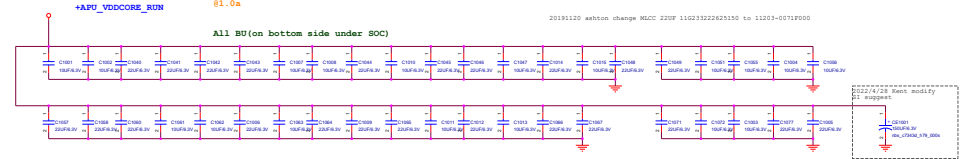
BO (Bottom side outside SOC)
BU (on bottom side under SOC)



Main Board

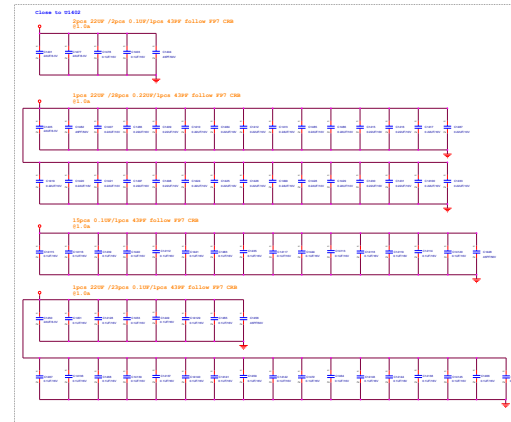
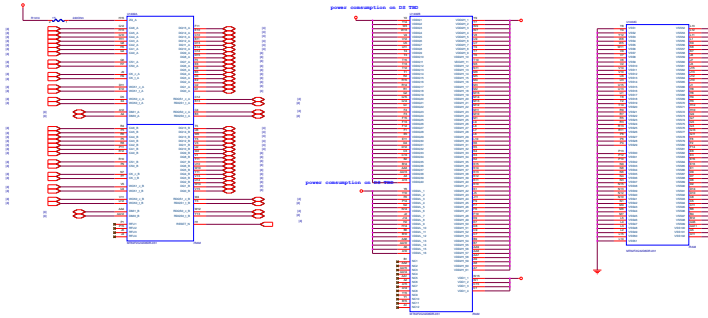
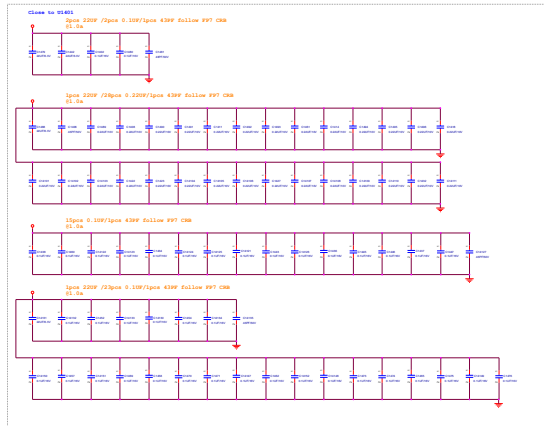
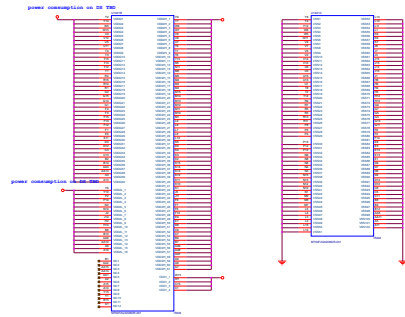
BO (Bottom side outside SOC)
BU (on bottom side under SOC)

40pcs 100F /1pcs 180FF follow FP7 CRB
@1.0a

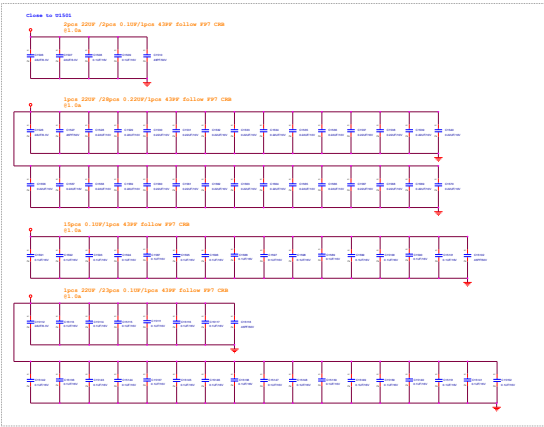
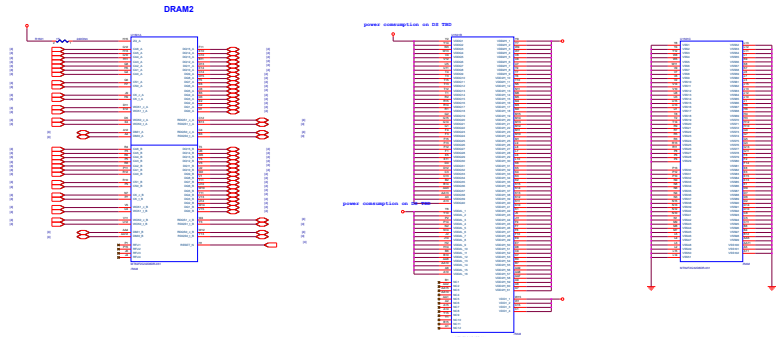


If the VSS plane is not to create a VDDIO_MEM_S3 plane, ceramic capacitors with NPO or COG dielectric are connected across the VDDIO_MEM_S3 and VSS plane split.

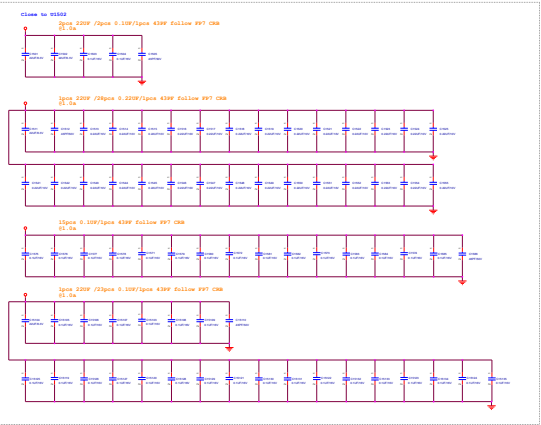
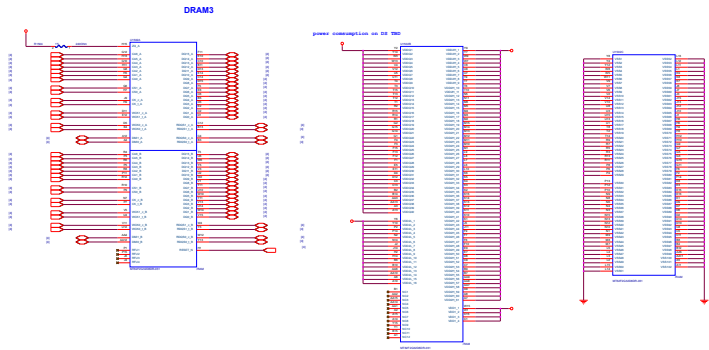
	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100
1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100	



LPDDR5 Channel C



LPDDR5 Channel D



Channel C	
Channel D	
Channel E	
Channel F	
Channel G	
Channel H	
Channel I	
Channel J	
Channel K	
Channel L	
Channel M	
Channel N	
Channel O	
Channel P	
Channel Q	
Channel R	
Channel S	
Channel T	
Channel U	
Channel V	
Channel W	
Channel X	
Channel Y	
Channel Z	

CPU_USB

20210305 CHIEHYIN change USB2.0 port , USB C0 for USB C port A, USB C1 for USB C port (USB C0/1 support USB4.0), USB B5 for typeA

- USB Port0 Type-C Port0
- USB Port1 Type-C Port1
- USB Port2
- USB Port3 BT
- USB Port5 Type-A Port5
- USB Port6 FP

[47]

[47]

[47]

[47]

[47]

[47]

[47]

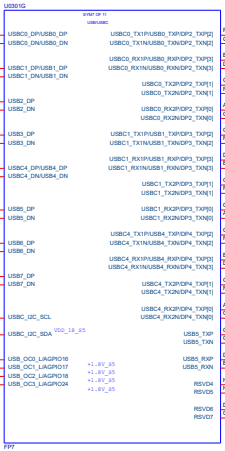
[47]

[47]

[47]

[47]

[47]



AMD Design check

ADP1013. If unused, enable internal pull down by software.



Add @20190829A

USB3.0 TX/RX
I/O-IOVPP5-D_VDDP (\$S_0.75)_FP6 (FDS)

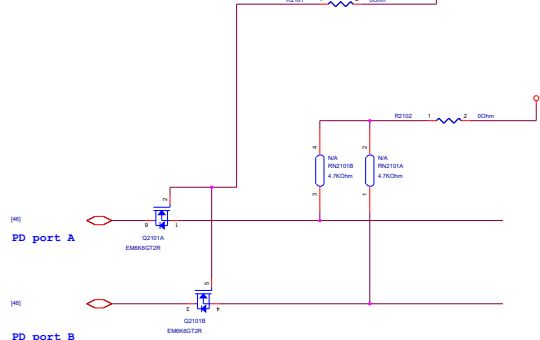
USB3.2 Gen2/USB4.0 USB-C Poart A

USB3.2 Gen2/USB4.0 USB-C Poart B

USB3.2 Gen2 Type-A

USB Port 0,1,4,5
USB-A USB3.2 Gen1(5Gbps): 304.8mm (12000mil)
USB-C USB3.2 Gen1(5Gbps): 177.8mm (7000mil)
USB-A & USB-C USB3.2 Gen2(10Gbps): 152.4mm (6000mil)

USB SDA/SCL level shift change +1.8VS
20200901 ashton modify



reserve I2C3 Isolater follow CRB 20211025

Project Name		Rev
ASUS FX505DY		R1.0
Title :		
Size	Dept.: NB-62-R03	Engineer:
Date: Wednesday, January 18, 2023	Sheet	21 of 104

The schematic diagram illustrates the SPI ROM circuit. It features a W74M25JWZEIQ SPI ROM (U2801) connected to a 28F040 EPROM (T2808) via an SL2809 driver (D402). The ROM is also connected to a 28F040 EPROM (T2805) via a 28F040 driver (D402). The circuit includes various resistors (R2805, R2812, R2813, R2814, R2815) and capacitors (C2809, C2801, C2810, C2811) for timing and signal conditioning. The ROM is connected to a 28F040 driver (D402) which is connected to a 28F040 EPROM (T2805). The circuit is powered by a 5V supply and ground.

[30,56,69]



[30,59,60,90]

[30,59,60,90]



[80]

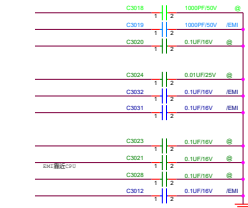
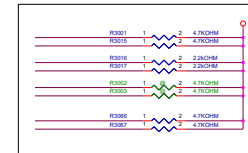
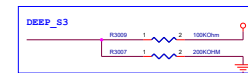
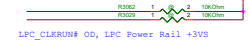
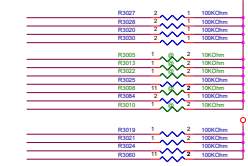
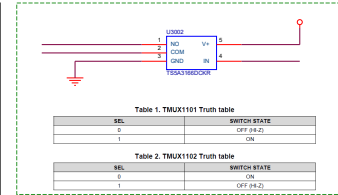
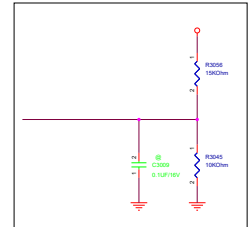


[6]

EC Power

VCC => +3V8 system power ; LPC
VSTBY=>+3VA_EC ;Power supply of EC power

20191205 additon change C3003 for placement

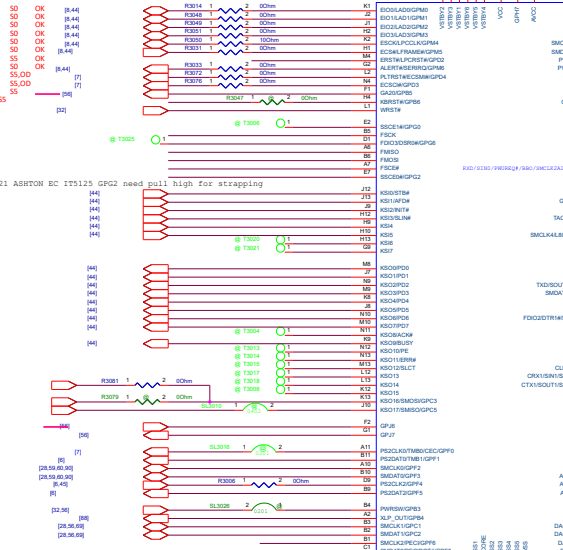


```
20191121 ASHTON R3027 R3028 R3030 remove
20191205 ashton remove R3011 R3057 R3064 Dohm
20200312 ashton del R3023, R3026, R3033, R3042, R3047, R3031, R3055
«Variant Name»
```

		Project Name FXS05YD		Part R1.0	
Title :					
Size C		Dept.: NS-SZ-PCG3		Engineer:	
Date: Wednesday, January 10, 2023			Sheet 30 of 104		

201911205 ashton R3014 R3048 R3049 R3050 change 0402
20210309 chiefyin R3014 R3048 R3049 R3050 change to John follow PP7 CR

20191121 ASHTON EC IT5125 GPD2need pull low for strapping



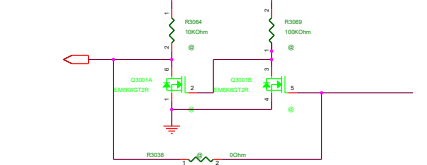
20200213 ashton modify SMB2 only test point

```

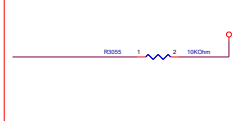
PW_FWRDTH# FO OUTPUT修改为 1.8V level for F97
AND_SF1_1 G6 INPUT修改为 1.8V level for F97
AND_SF1_2 F4 INPUT修改为 1.8V level for F97
AND_SF1_3 G6 INPUT修改为 1.8V level for F97

```

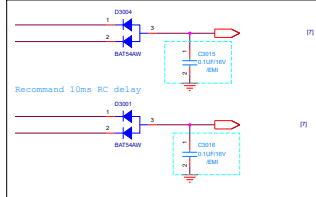
LEVEL SHIFT



20210319 chiehyin FP7 change to PU 1.5V



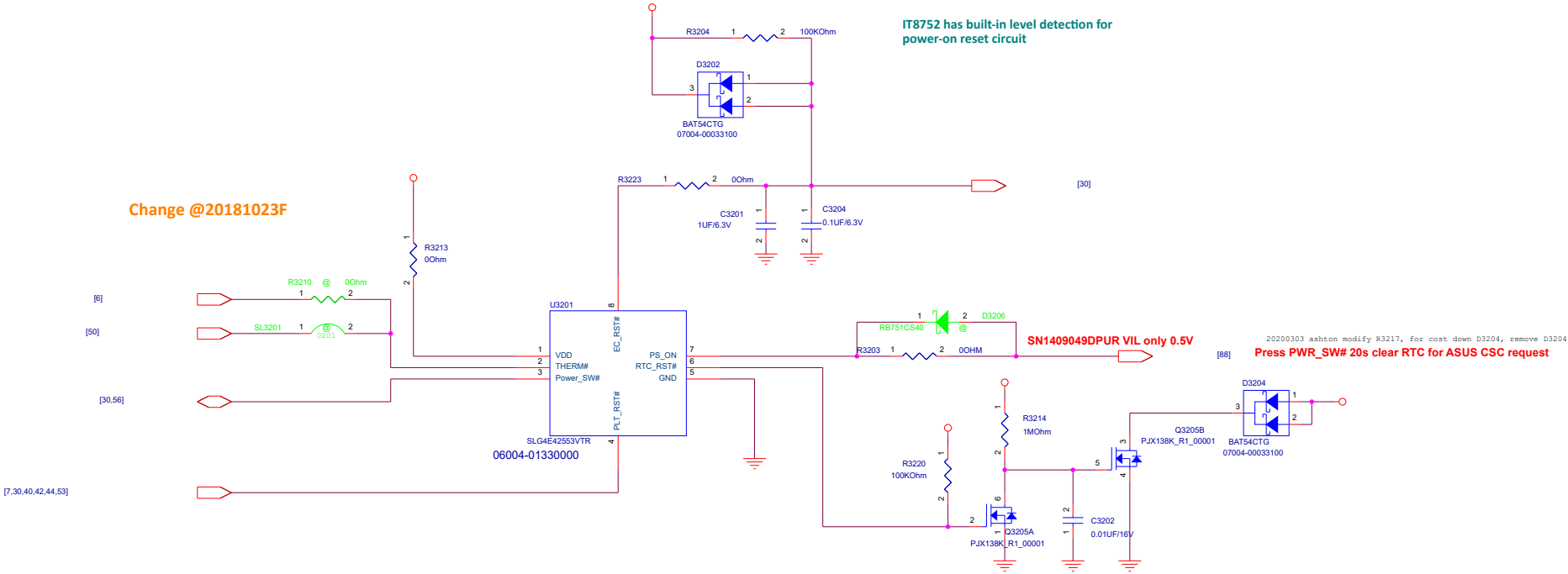
for load code



Modern standby project should use Silego solution for EC/RTC reset (Microsoft hardware requirements)

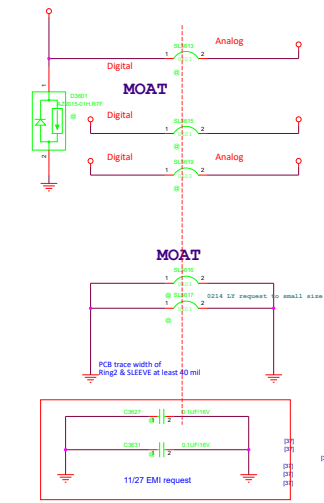
6.6.2 Power button behavior

<https://docs.microsoft.com/en-us/windows-hardware/design/minimum/minimum-hardware-requirements-overview#section-60---shared-minimum-hardware-requirements-for-components>
UX362FA R1.3 board will verify this circuit 7/E



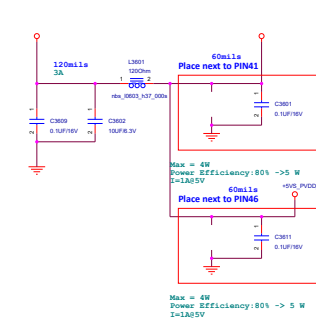
<Variant Name>

		Title :	RST_Reset Circuit
ASUSTek COMPUTER INC. N84		Engineer:	NR EE RD3
Size B	Project Name FX505DY		Rev R1.0
Date: Wednesday, January 18, 2023		Sheet	32 of 104



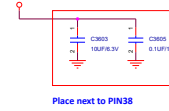
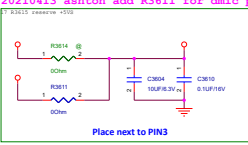
20210414 ashton change BAPD to U3601 Pin42
BAPD Pin 1 by web table define

AZ_B-AUD-S (S5_1.8)_FP6 (FDS)

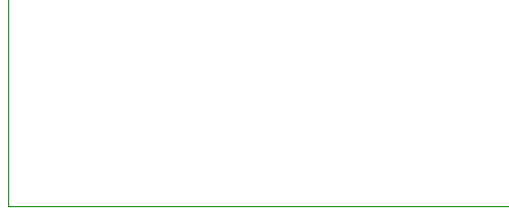
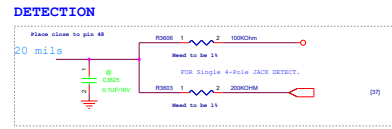


20191216 ashton remove R3617
remove R3614 reserve +20V

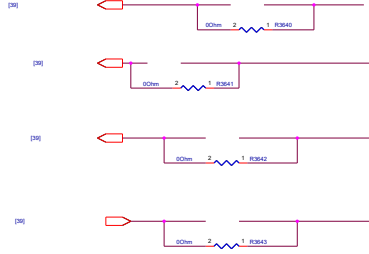
20210413 ashton add R3611 for dmic power rail optional



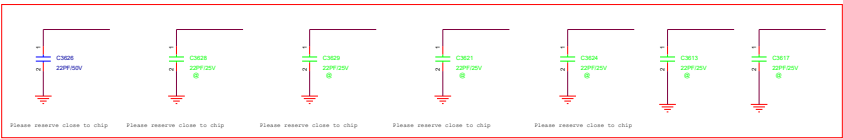
20191201 ashton remove R3604



20171228 modify level shifter for I2S follow ULT5408

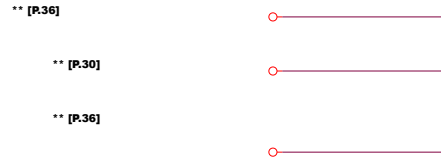


20210414 ashton change DMIC1 DATA34 to U3601 Pin1



Core Design		Project Name	Rev
ASUS		OX531GX	1.0
Title :		AUD ALC3288-CG	
Site	Dept.:	ASUSTek COMPUTER INC.	Engineer: EE
Date: Wednesday, January 18, 2023	Sheet	06	of 104

*** POWER

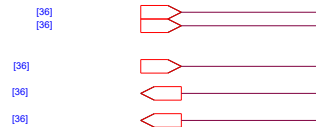


*** SINGAL

** Line to Codec [36]



** Headset from Codec [36]



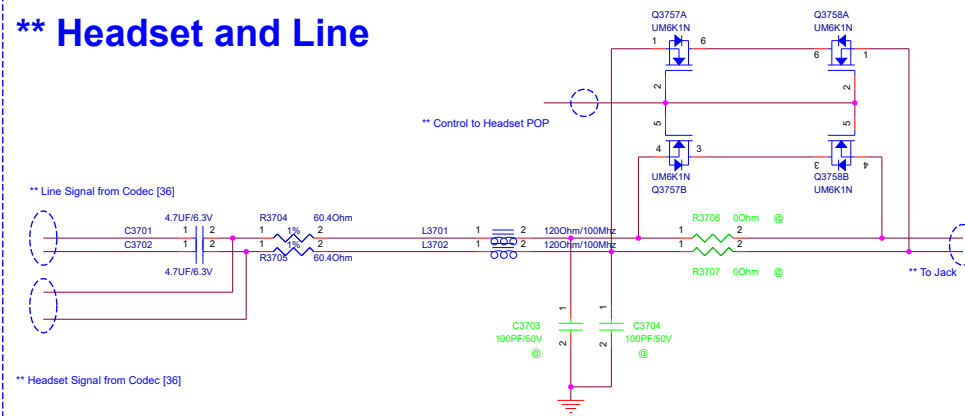
** Control Pin from Codec [36]



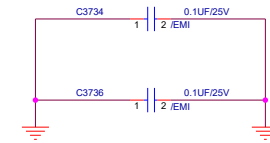
** Control Pin from APU [7]



** Headset and Line

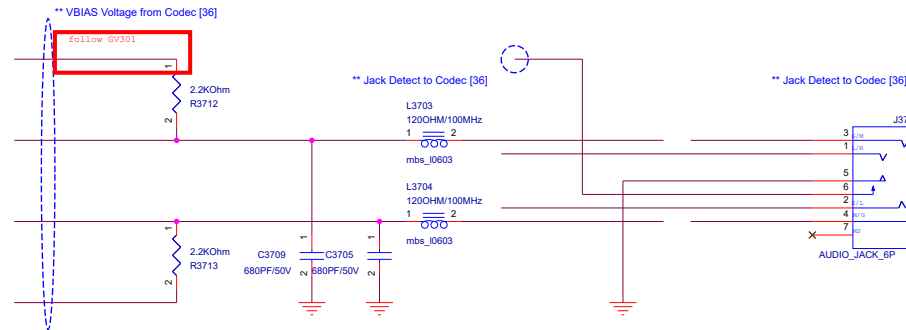


** A_GND / GND

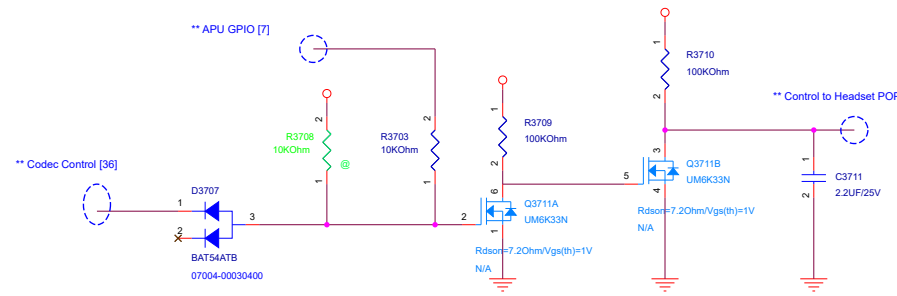


** Jack and MIC

Add more than 100pf cap for Headset detect



** TVS

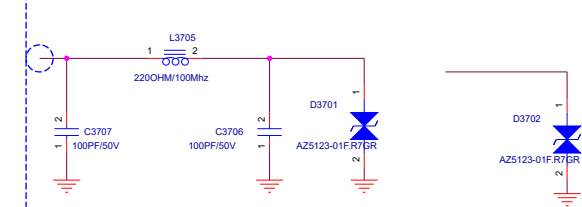


20210413 ashton change Q3711 Vgs=1V for DVDD 1.8V

** TVS

HP & MIC Connector

HP ESD Protect



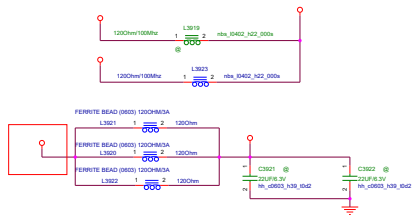
Design IP 0419 選用 07024-01152200 EOL
故使用 07024-01152200 ESD

EXTERNAL MICROPHONE



ASUS		Project Name	Rev
Title : AUD_EXT Jack		R1.2	
Size B	Dept.: ASUSTeK COMPUTER INC	Engineer: EE	
Date: Wednesday, January 18, 2023	Sheet	37	of 104

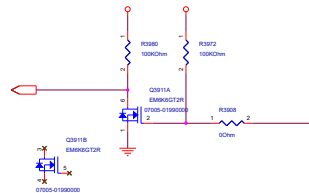
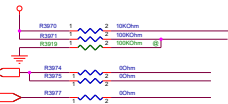
Check power V5/V5U5



[7]

[7]

[8]



AMD platform: I2C

Left

Right

AD1	AD0	W	R	ADDR
0	0	0x80	0x81	0x40
0	1	0x80	0x83	0x41
1	0	0x84	0x85	0x42
1	1	0x86	0x87	0x43

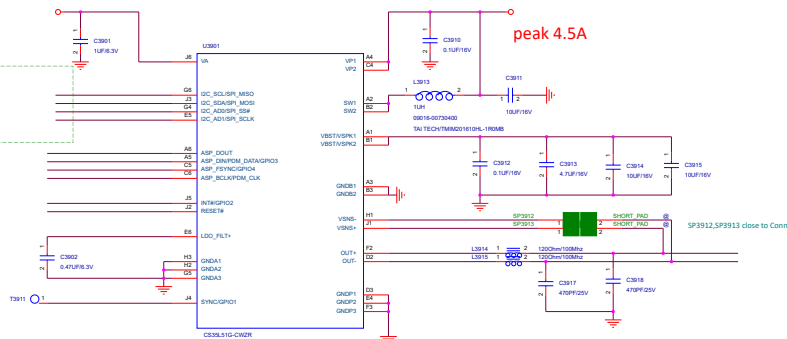
0=GND 1=VA

Check APU I2C Power Domain!!!

I2C Address Table

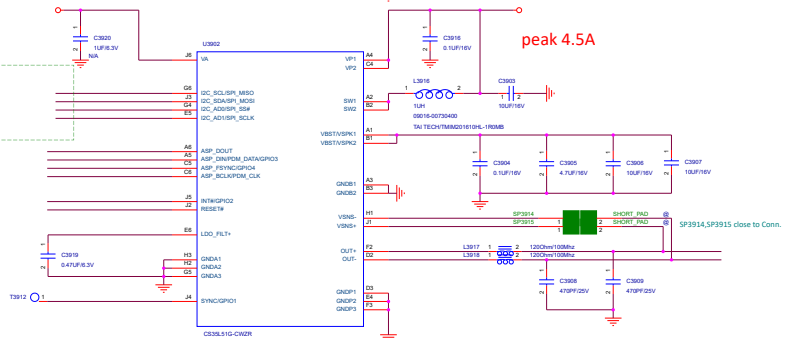
	Address 8bit	Address 8bit
L	Write: 0x80	Read: 0x81
R	Write: 0x82	Read: 0x83

Intel platform: SPI
AMD platform: I2C



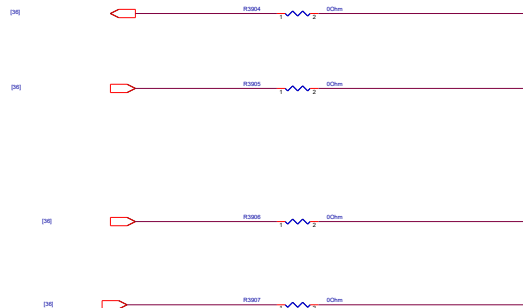
peak 4.5A

Intel platform: SPI
AMD platform: I2C



peak 4.5A

Check level shift

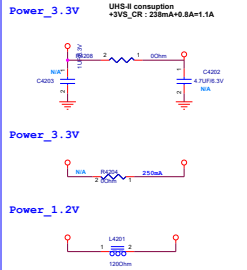


Main Speaker Connector

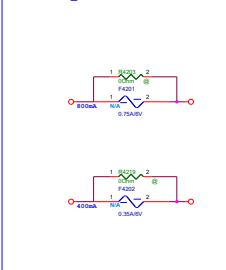


ASUS		Project Name	Rev
Title : AUD_INT_SPK			R1.0
Size	Dept. : ASUS&A COMPUTER INC.	Engineer: EE	
Date: Wednesday, January 18, 2023		Sheet 06 of 103	

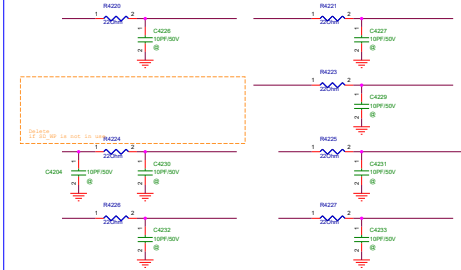
Power



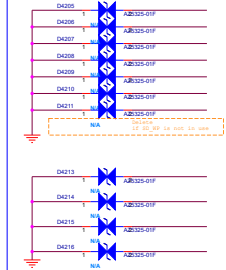
Safety



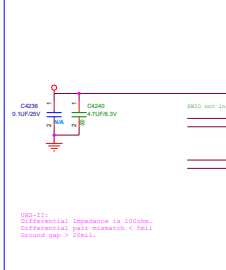
EMI



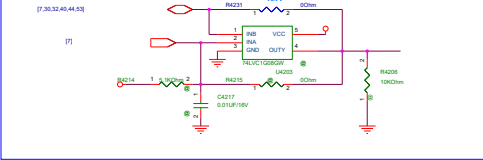
ESD



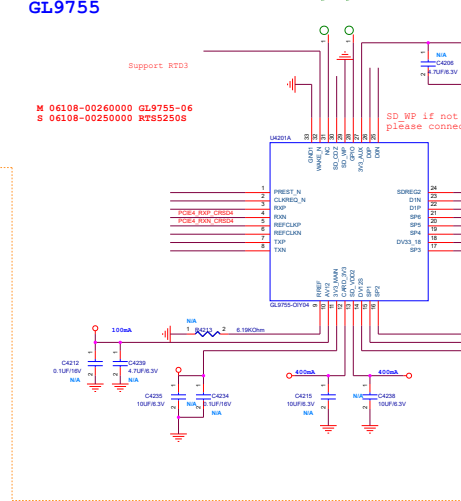
Micro SD Connector



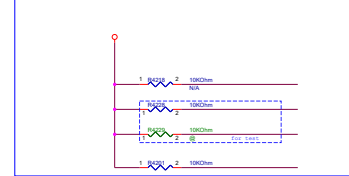
Reset



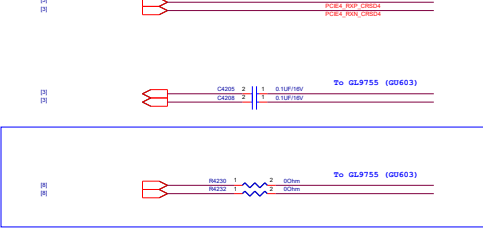
GL9755

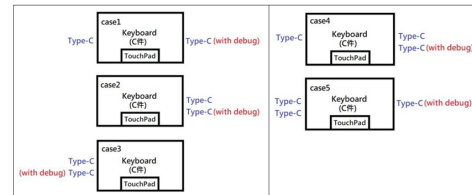
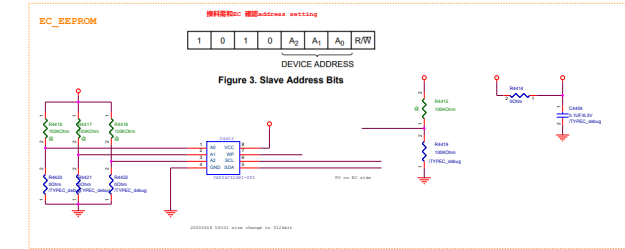
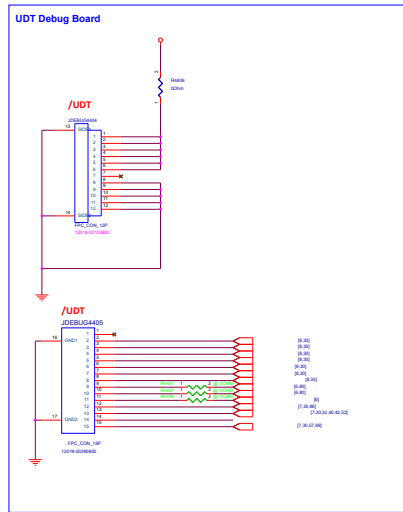


Pull UP



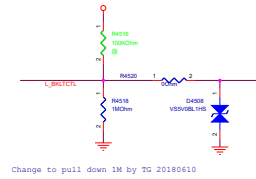
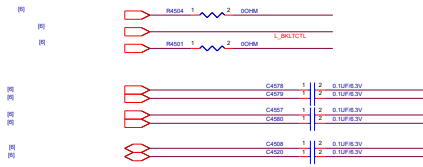
SD HW option





		Title : DEBUG_LPC	
AsusTek COMPUTER		Engineer: NR EE RD3	
Size	Project Name		
Custom	GX502GX		
Date	Model/Rev. /Date	Drawn	Appr
10/10/11	10/10/11	10/10/11	10/10/11

eDP_BL PWM

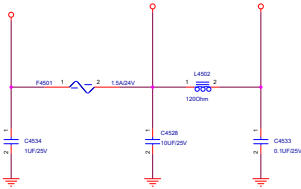


Change to pull down 1M by TG 20180610

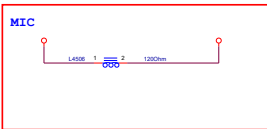
eDP_HP_D (CPU)

Panel BL Power

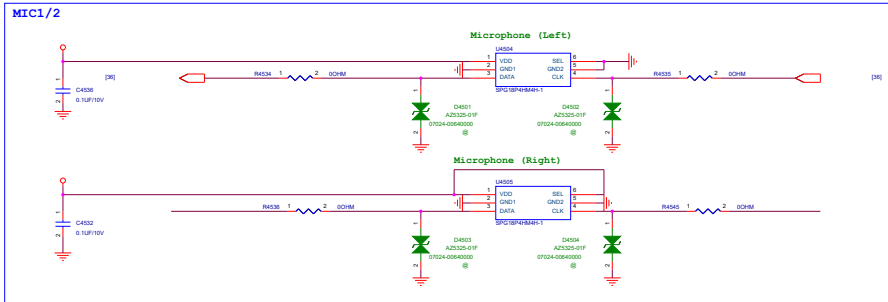
20200221 addbus change only polyswitch



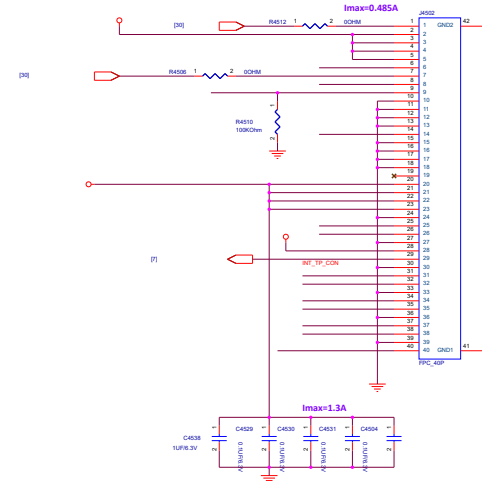
Display Panel
O-I018-S (S0_1.8)_FP6 (FDS)



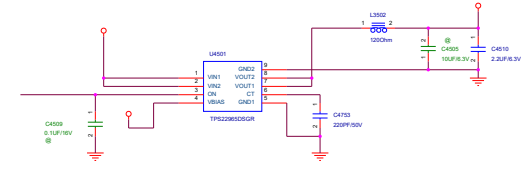
MIC1/2



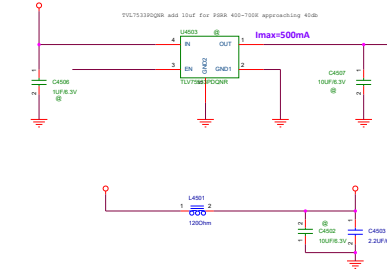
eDP Panel Conn.



+3VS_LCD [For Panel]



+3VSUS_TP [For Touch]



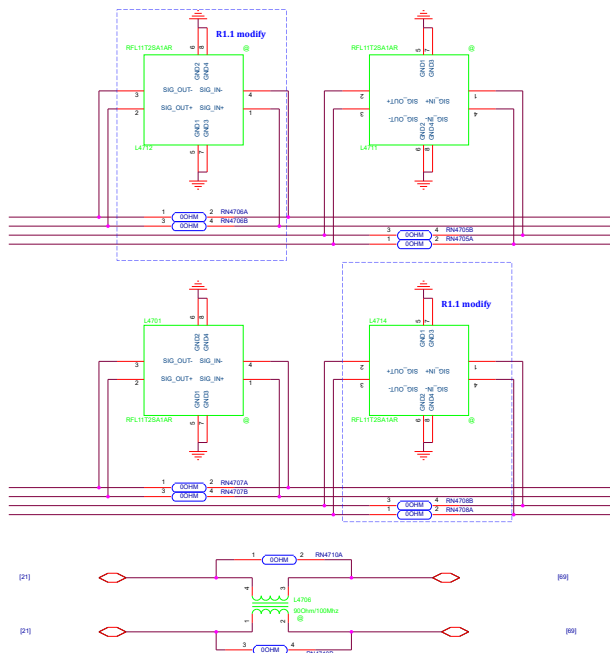
©Core Design

ASUS		Title : CRT_eDP	
ASUS Fan COMPUTER		Engineer: NR EE RD3	
Rev	Project Name	Custom	Rev
		GX502GX	1.0
Date: Wednesday, January 18, 2023		Page: 45 of 100	

USB3.0 EMI

EMPASS footprint 通用
Check 上標: nbs_filter_6p_001c
消磁上標: nbs_filter_6p_p4_001c

20191202 ashton L4711 / L4712 swap



NOTE 8. PIN ASSIGNMENT (FRONT VIEW)

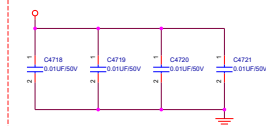
Pin No.	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
	GND	TX1+	TX1-	V _{BUS}	CC1	D+	D-	SBU1	V _{SS}	RX2-	RX2+	GND
Pin No.	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1
	GND	RX1+	RX1-	V _{BUS}	SBU2	D-	D+	CC2	V _{SS}	TX2-	TX2+	GND

NOTE 9. LASER WELD POINTS MAY BE DISCOLORED.

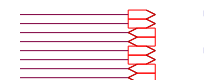
Irat=6A / 0603



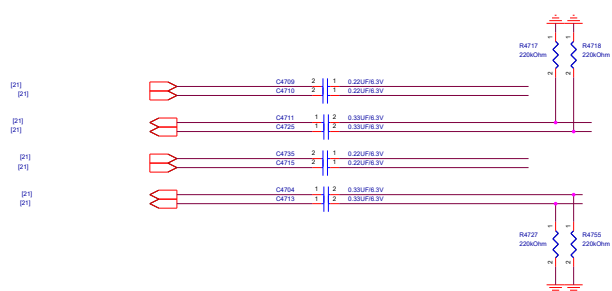
20190702
VBUS capacitor, Close to Connector for VBUS1 to VBUS4



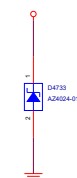
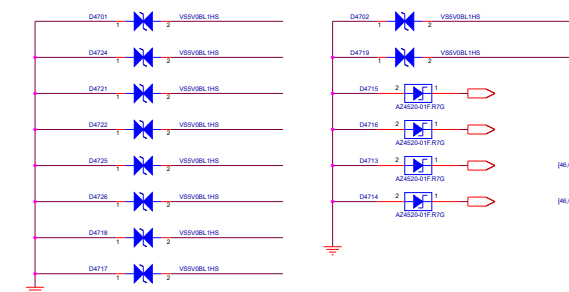
TYPE-C Connector



TYPE-C PORT A



USB3.2/USB2.0/SBU/CC
ESD-Protection



Project Name		Rev
Type-C_ALT_USB3-10G + DP + PD + Slave_Charger_T1		2.0
Title : USB3.1 TYPE-C+T1 1046A		
Size	Dept.: ASUS/IN COMPUTER INC.	Engineer: NR EE RDS
Date: Wednesday, January 16, 2023	Sheet	47 of 104

ALERT/SDA/SCL: Open-drain output; pullup resistor 5Kohm

Pin function Supply voltage.: 1.62 V to 3.6 V

Pin function Supply voltage.: 1.62 V to 3.6 V

SMBUS1 to EC



(30)

(30)

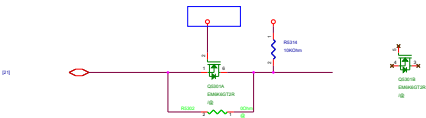


DEVICE TWO-WIRE ADDRESS	ADD0 PIN CONNECTION	Output
1001000 90	Ground	CPU
1001001 91	V+	VRAM
1001010 92	SDA	GPU
1001011 93	SCL	

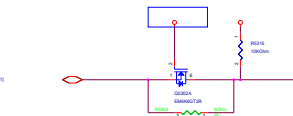
Control

WLAN card vendor recommend (Intel/Realtek)
1. Module internal PU
2. Placeholder for protect unconnected input

WLAN Ext_HW_Kill

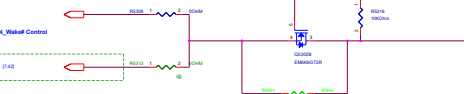


BT Ext_HW_Kill



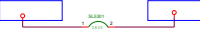
PCIE Wake

WLAN_Wake# Control

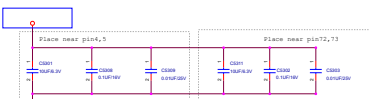


Power

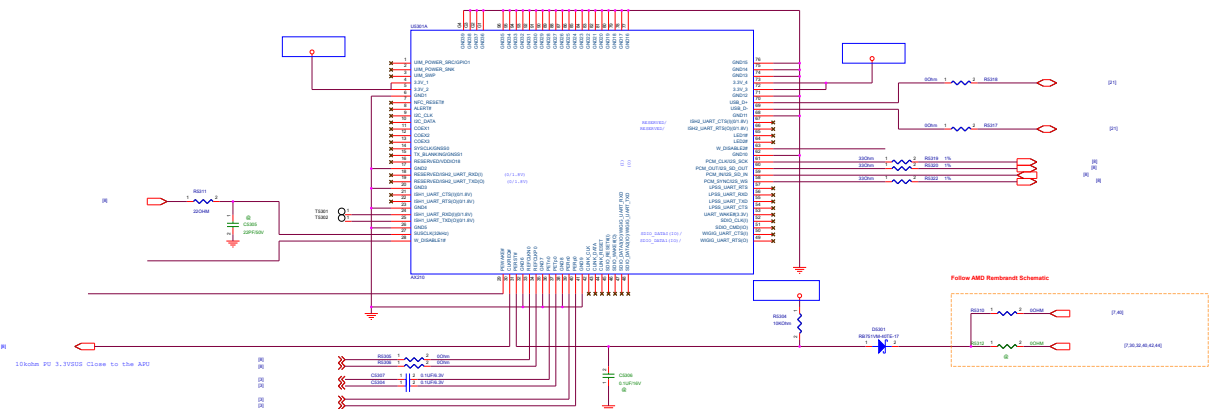
WLAN PWR_+3V_NGFF_WLAN (Non-ISCT)
Support ASUS Open Cloud Computing (AOConnect)
WLAN PWR to +3VSD5



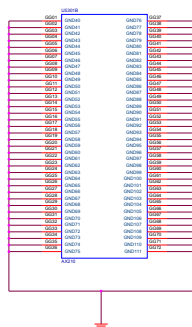
Bypass capacitor



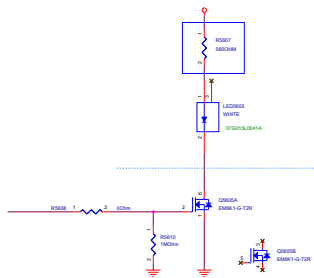
For EMI

**AX210**

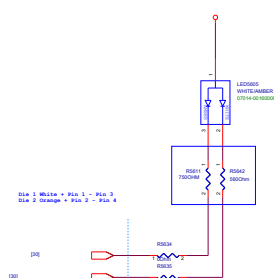
AX210 GND



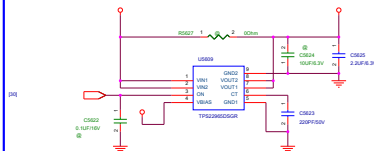
PWR LED (GU603)



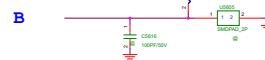
Charger LED (GU603)



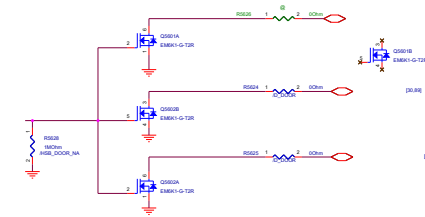
小板+5VSUS



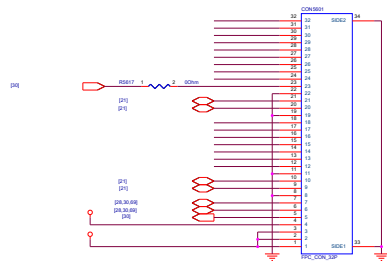
B鍵 (Maximum rating 12V/50mA) (Minimum rating 1V/10uA)



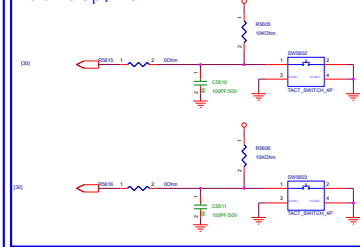
D Door(為了讓CON5601多一根GND)



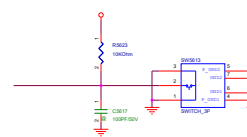
Connect to Left Board (page 71)



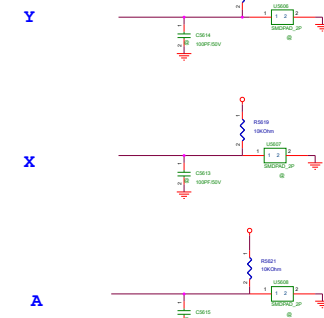
Volume Up / Down



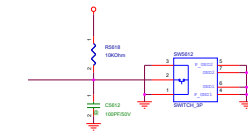
L1 (Maximum rating 12V/50mA) (Minimum rating 1V/10uA)



YXA鍵 (Maximum rating 12V/50mA) (Minimum rating 1V/10uA)



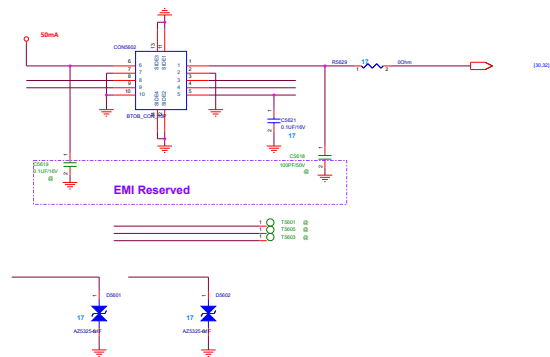
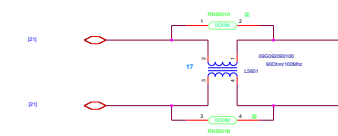
R1 (Maximum rating 12V/50mA) (Minimum rating 1V/10uA)



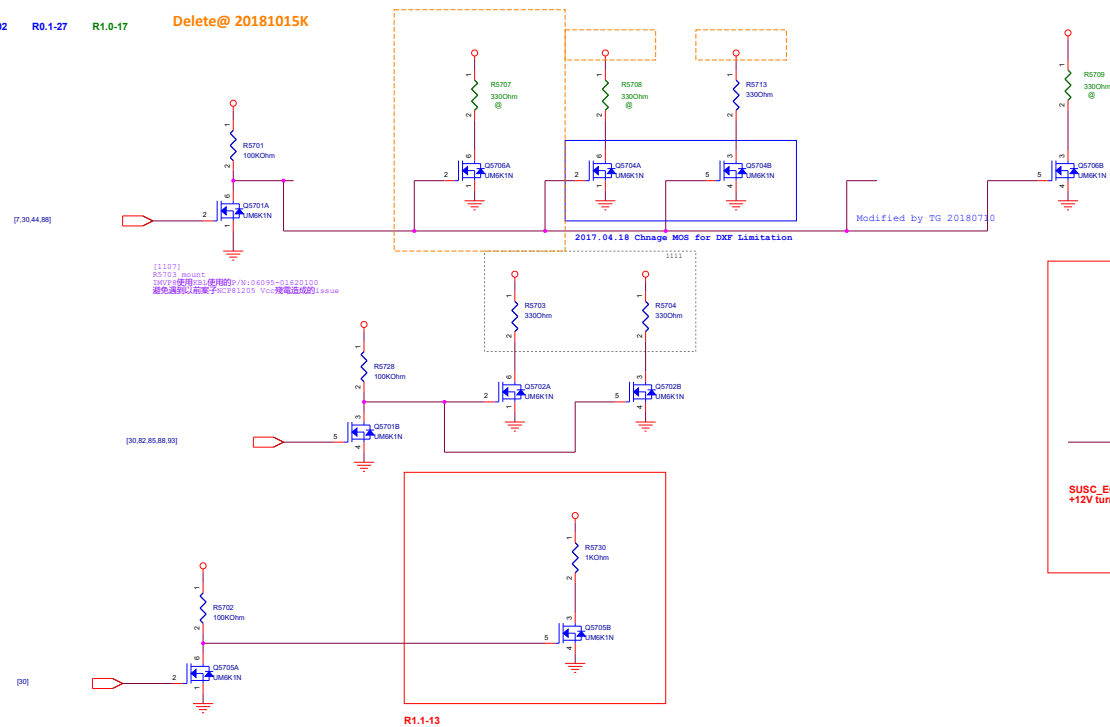
Power Key and FigerPrinter (GX703)



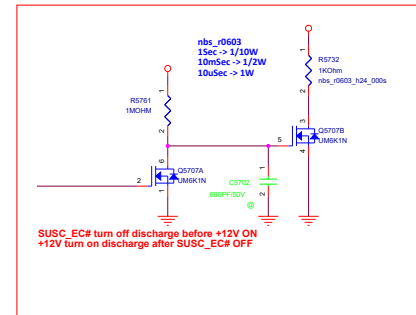
S	OE	Function
X	H	Disconnect
L	L	D=1D
H	L	D=2D



R0.1-02 R0.1-27 R1.0-17 Delete@ 20181015K



Change DSW to SUS
@20181009



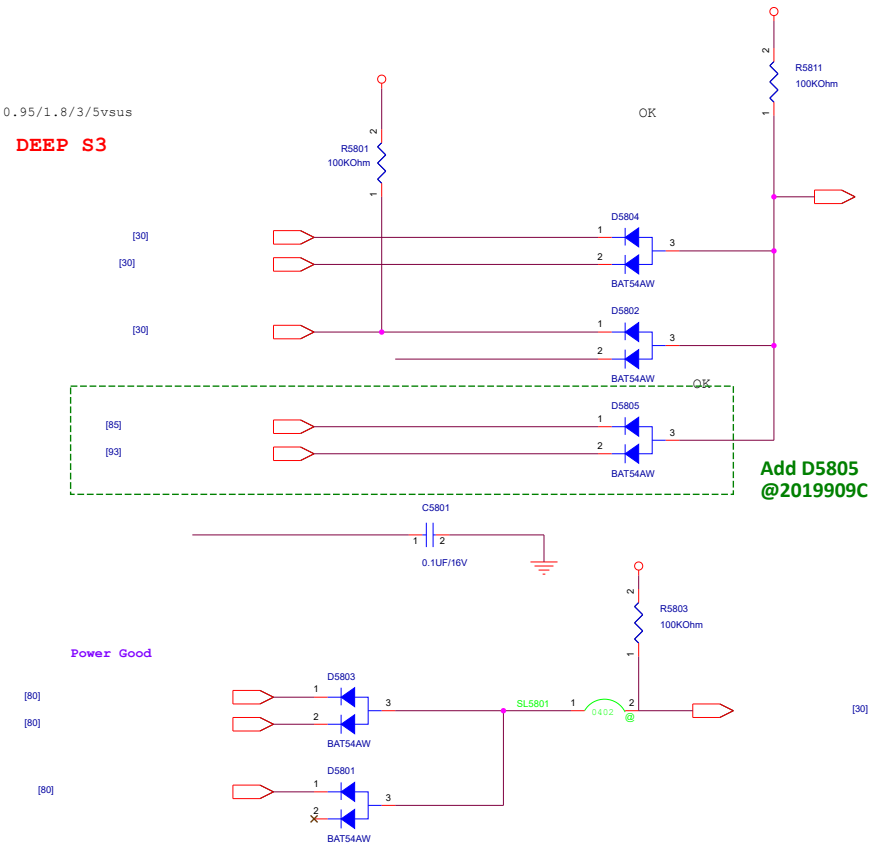
<Core Design>

		Title : DSG_Discharge	
ASUS Toki COMPUTER		Engineer: NR EE RD3	
Size Custom	Project Name GX502GX	Rev 1.0	
Date: Wednesday, January 18, 2023	Sheet	57	of 104

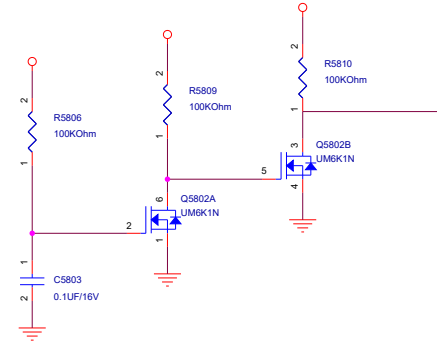
POWER GOOD DETECTOR

0.95/1.8/3/5vsus

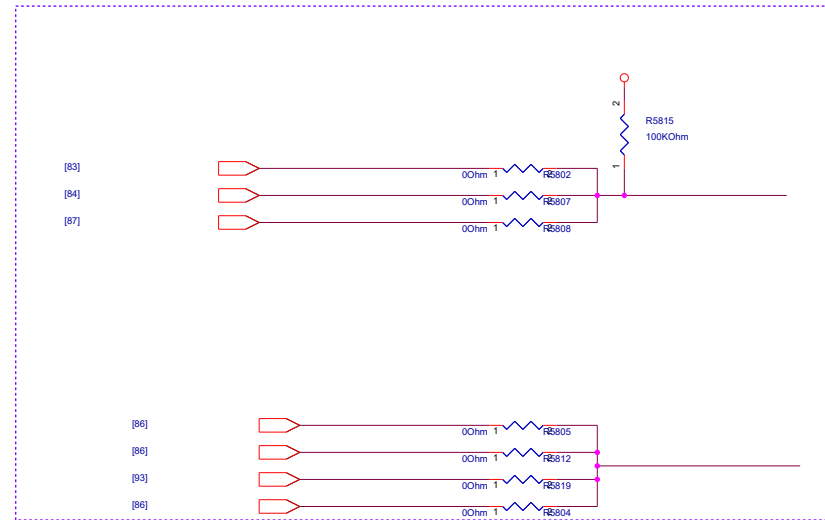
DEEP S3



[30]

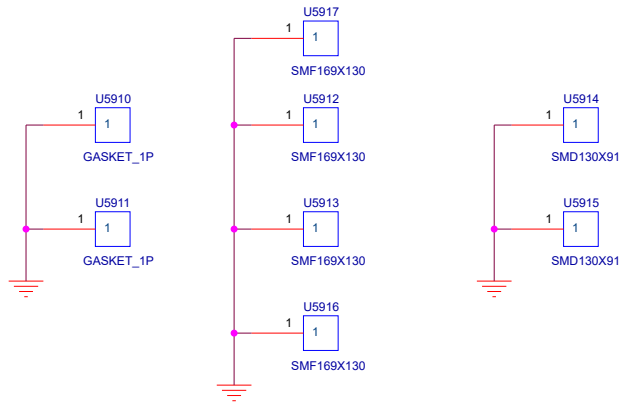
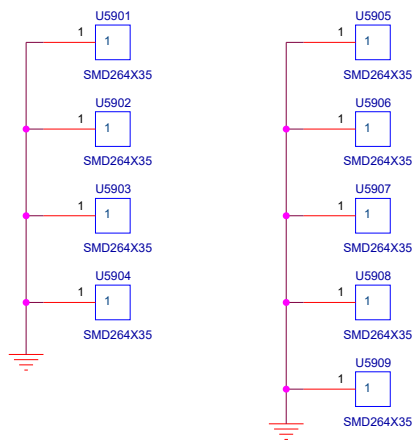


Power Good

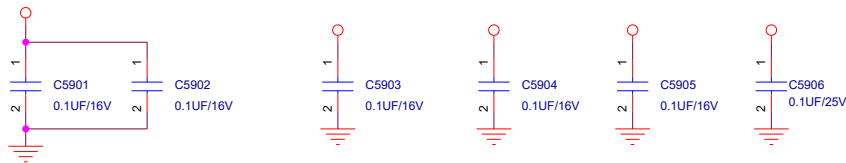


ASUS		Project Name	Rev
		FX505DY	R1.0
Title : POWER GOOD DETECTOR			
Size	Dept.:	ASUSTek COMPUTER INC.	Engineer: NR EE RD3
B			
Date: Wednesday, January 18, 2023	Sheet	58	of 104

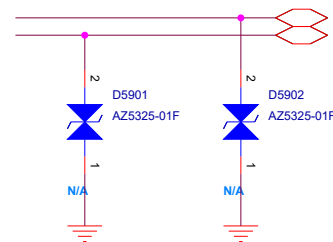
Clip



EMI



close to J6003

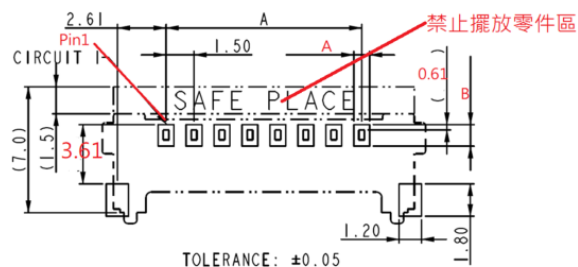


[28,30,60,90]
[28,30,60,90]

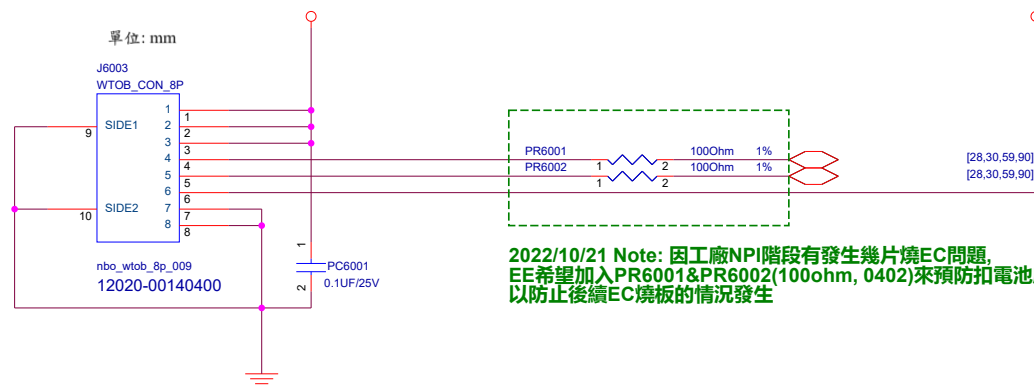
<Core Design>

ASUS®		Title : OTH_EMI	
ASUSTeK COMPUTER		Engineer: NR EE RD3	
Size A	Project Name GX502GX		Rev 1.0
Date: Wednesday, January 18, 2023		Sheet 59 of 104	

Battery Connector



BAT :
40Wh
4S1P
1C能耐=2.584A
滿充電壓=17.8V
充電能力=1.1C=2.843A
放電能力=1.5C=3.724A



2022/10/21 Note: 因工廠NPI階段有發生幾片燒EC問題, EE希望加入PR6001&PR6002(100ohm, 0402)來預防扣電池所產生的突波, 以防止後續EC燒板的情況發生

Note: Battery Connector 正確性與BAT1_IN_OC#是否預留!

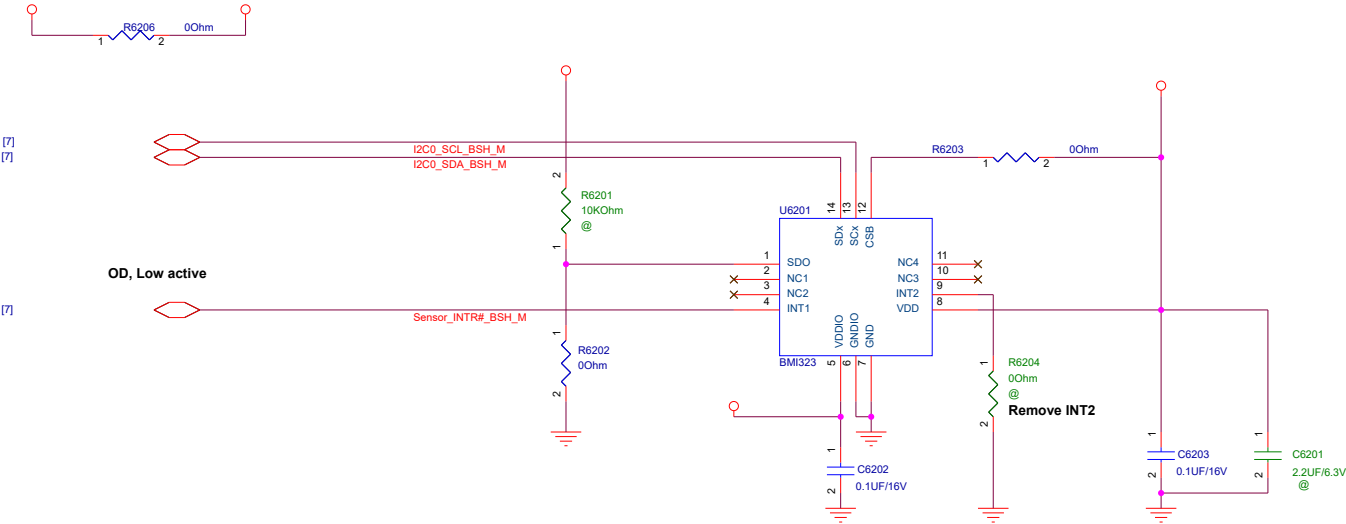
2022/6/22 Note: Follow需求修改Footprint為nbo_wtob_8p_008

2022/8/17 Note: Follow EE需求更換料號為12020-00140400, Footprint為nbo_wtob_8p_009

2022/8/31 Note: 12020-00140400 Footprint nbo_wtob_8p_009加入鐵片後推禁制區

Project Name GV301		Rev R1.0
Title : DC & BAT IN		
Size A4	Dept.: NB_Power team	Engineer: NR EE RD3
Date: Wednesday, January 18, 2023	Sheet 60	of 104

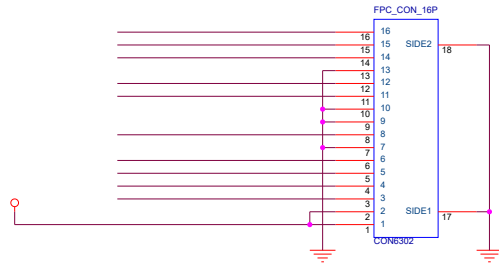
BMI323



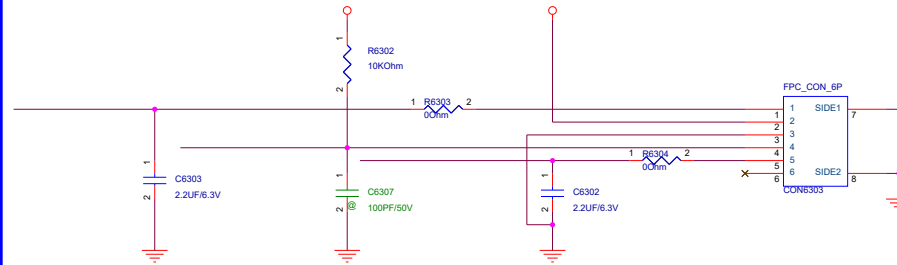
<Variant Name>

ASUS®		Title : BSH_Sensor	
ASUSTeK COMPUTER		Engineer: NR EE RD3	
Size Custom	Project Name GL752VW		Rev 1.0
Date: Wednesday, January 18, 2023		Sheet 62	of 104

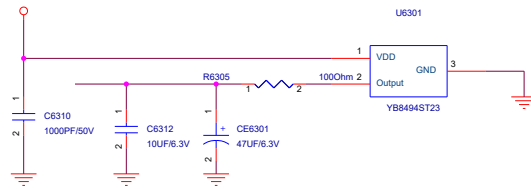
Connector LeftBoard(P71)



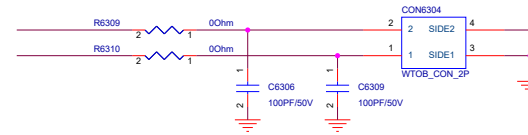
Right Joystick connector (Maximum rating 5V/1mA) (Minimum rating 3.3V/60μA)



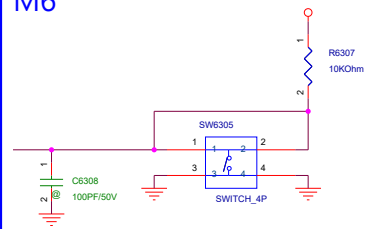
R2



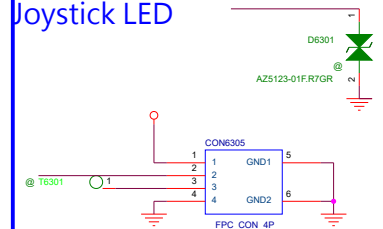
Right Vibrator connector (Maximum rating 5V/0.55A)2022/8/15



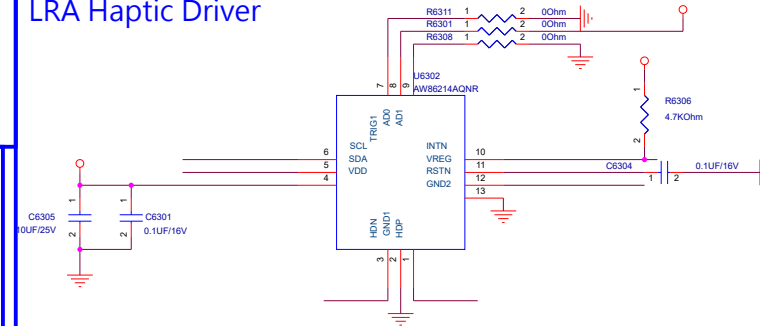
M6



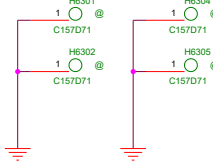
Joystick LED



LRA Haptic Driver



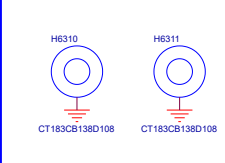
Hole 1



Hole 2



Nut 3

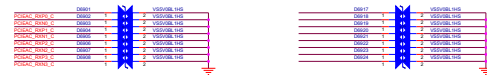
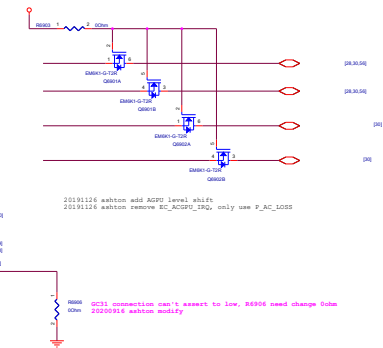


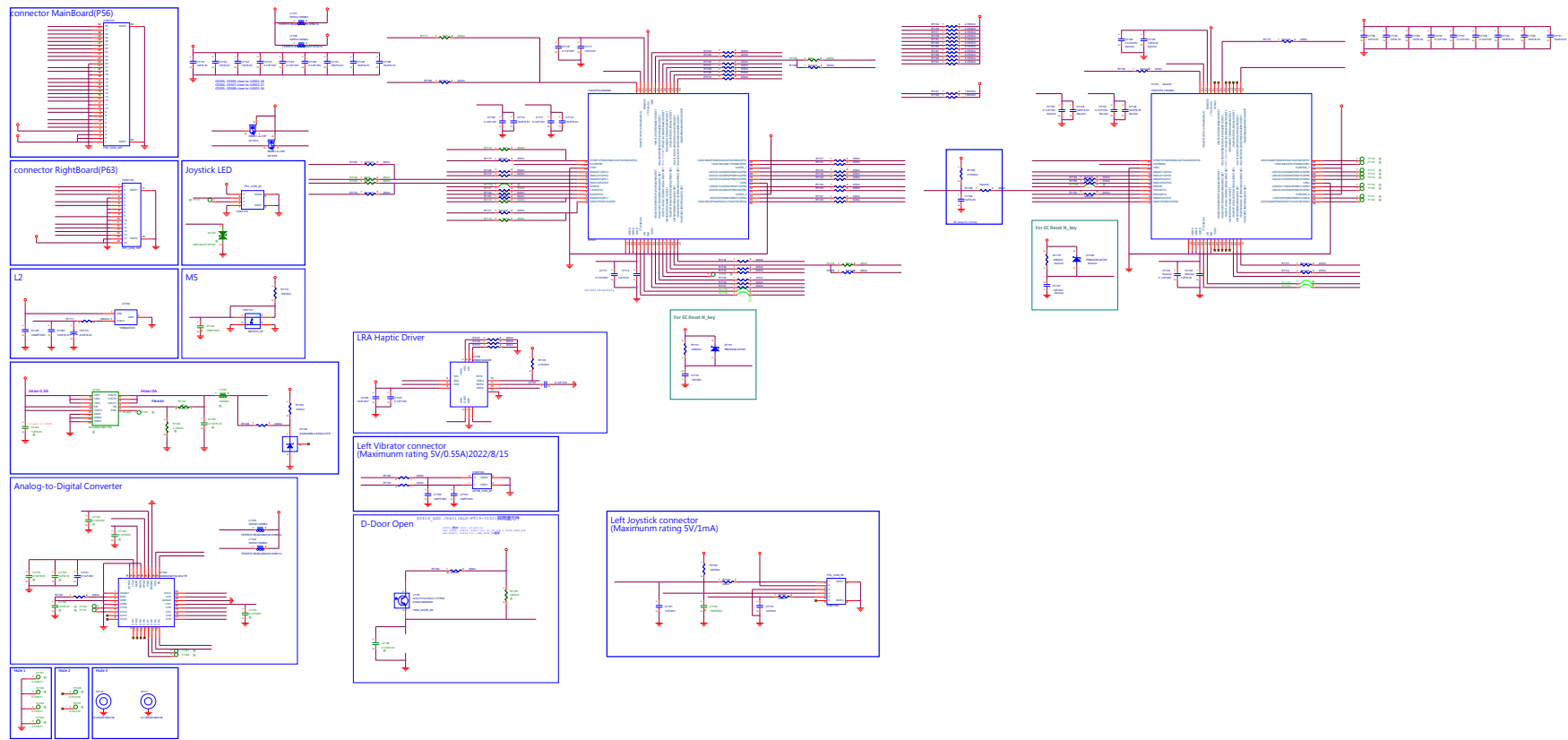
Hole 4



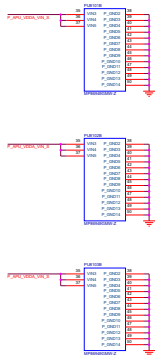
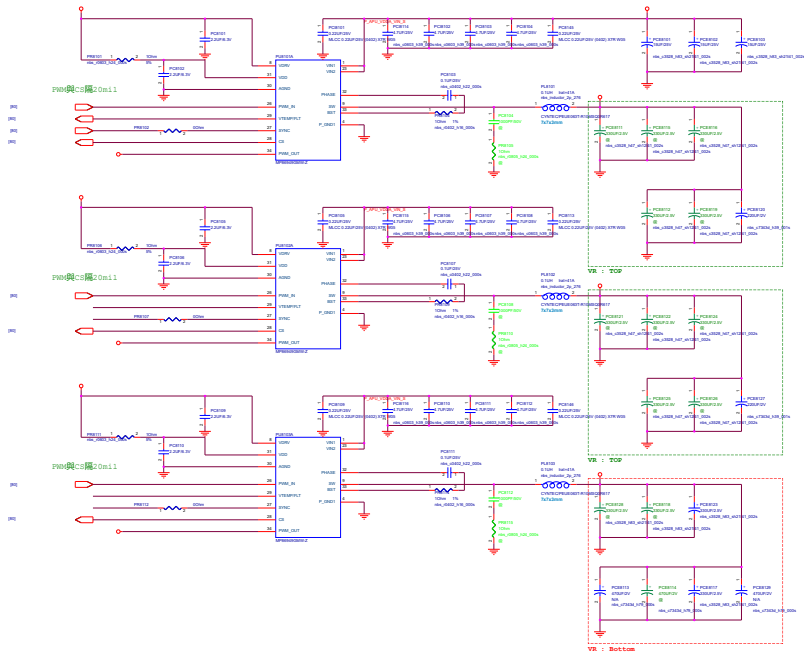
<Variant Name>

ASUS		Title : NGFF SSD(MAXIM)	
ASUSTek COMPUTER		Engineer: NR EE RD3	
Size Custom	Project Name GL752VW		Rev 1.0
Date: Wednesday, January 18, 2023		Sheet 63 of 104	

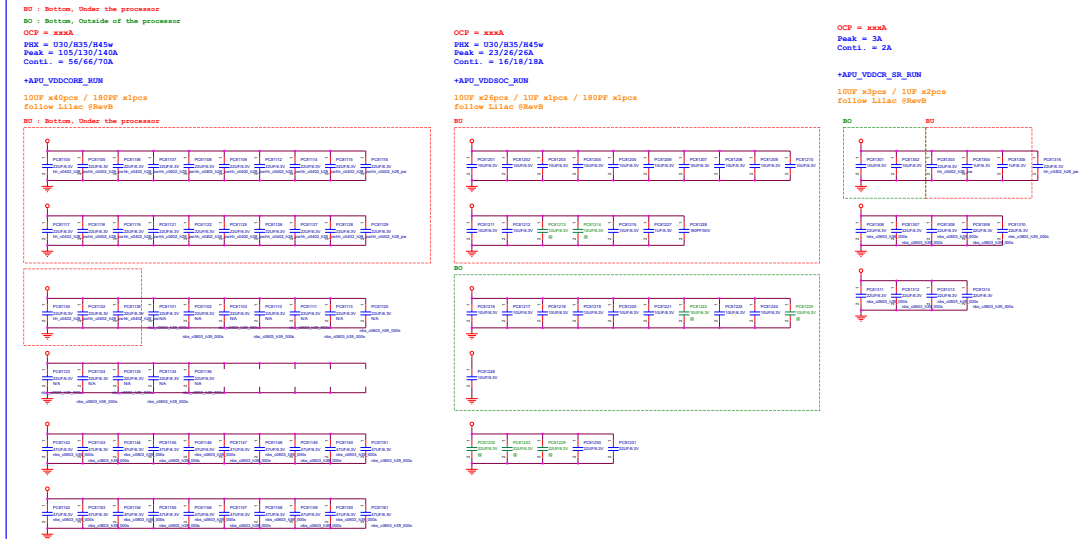
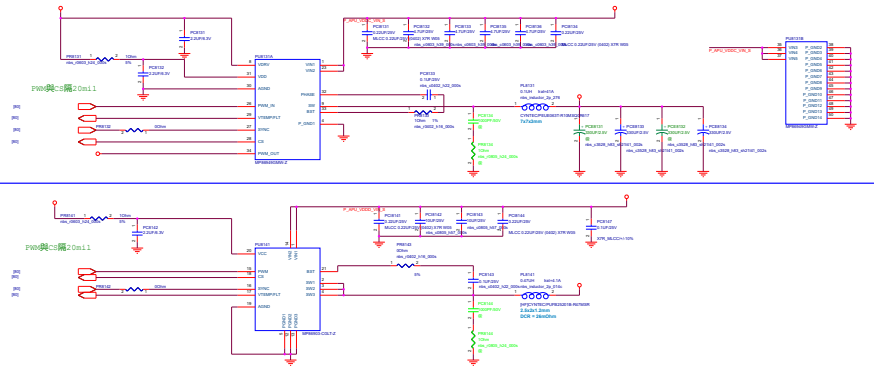




+APU_VDDCORE_RUN



+APU_VDDCH_RR_RUN

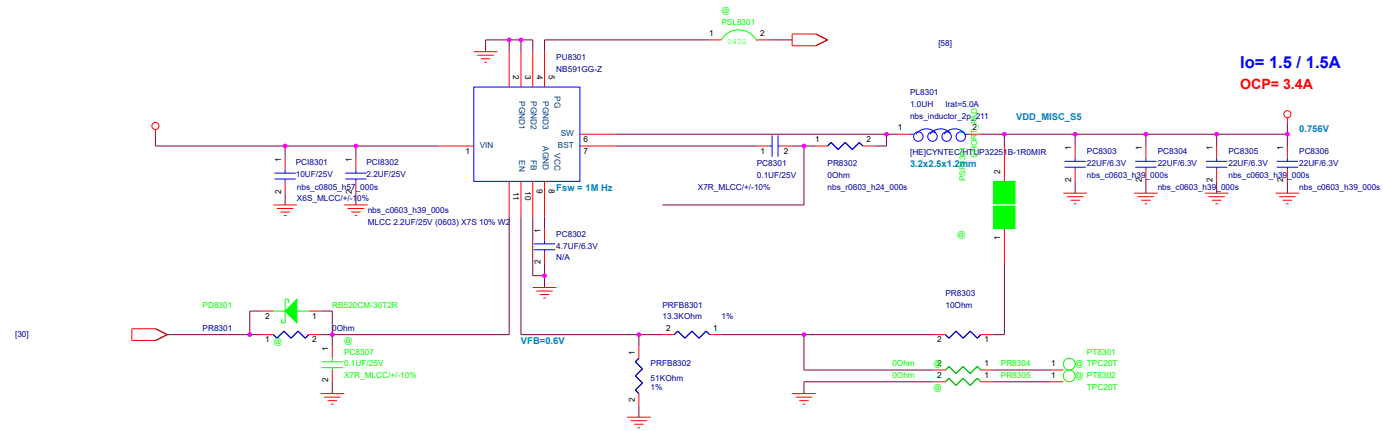




[6]
[6]

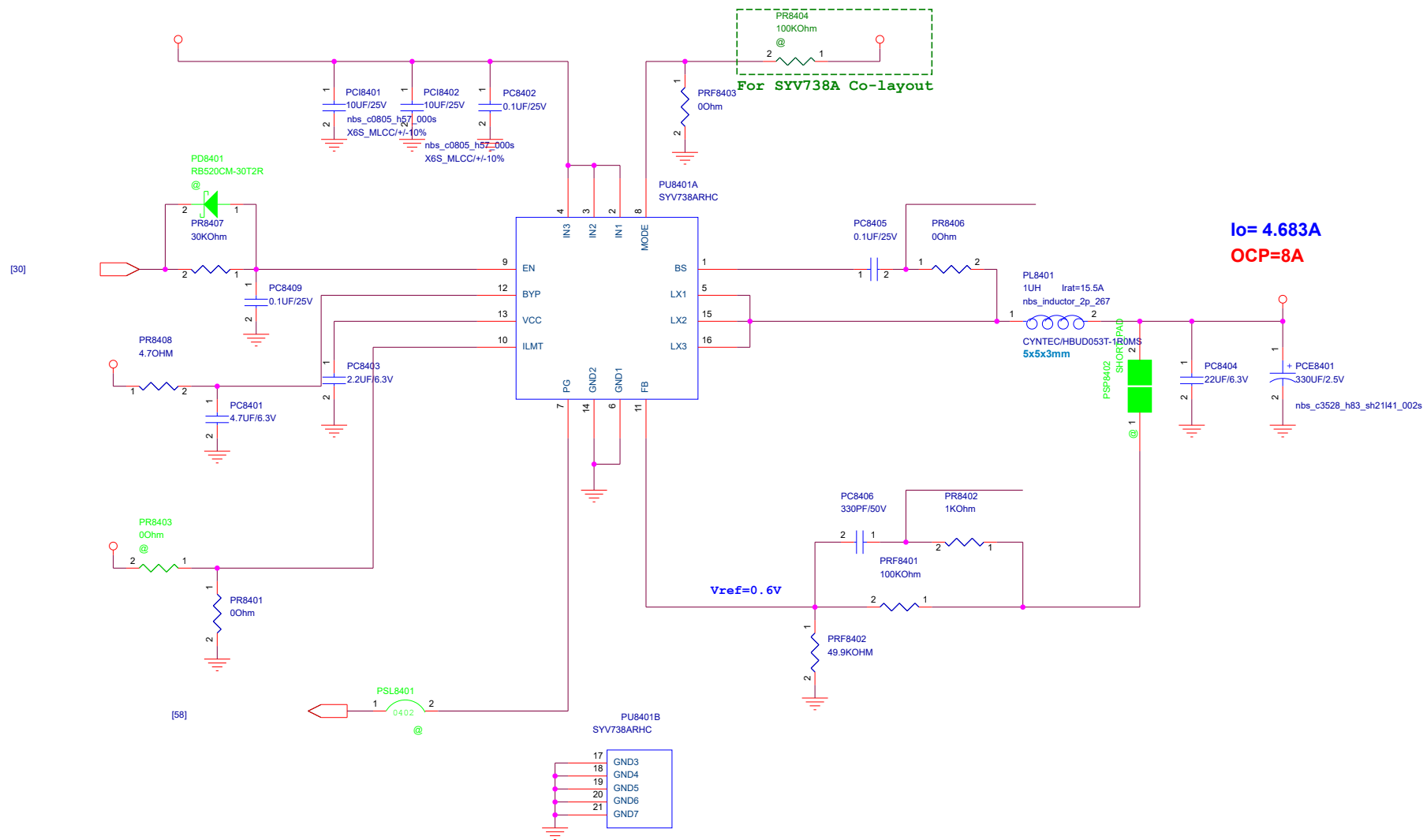
		Project Name		Rev
		GA503QS		R1.0
Title : PW_+0.75VS				
Size	Dept:		Engineer:	
A3	NB Power team		CS Lin	
Date: Wednesday, January 18, 2023		Sheet	82	of 104

+0.75VSUS [For APU]



<Variant Name>		Project Name	Rev
		ASUS GA503QS	R1.0
Title : PW_FLOWCHART			
Size	Dept.:	Engineer: CS Lin	
A3			
Date: Wednesday, January 18, 2023	Sheet	83	of 104

PW_1P8VSUS [For GPU]



<Core Design>

		Project Name		Rev
		DESIGN_IP		R1.0
Title : PW_+1.8VSUS				
Size A4	Dept.: NB Power team		Engineer: Power	
Date: Wednesday, January 18, 2023			Sheet	84 of 102

30,57,82,88,93]

VDDMEM電壓	PHX=0.95V	RMB=0.75V (後改0.814)
PRF8502	84.5K	51K
	10G212845214010 N/A	10G212510214010 N/A



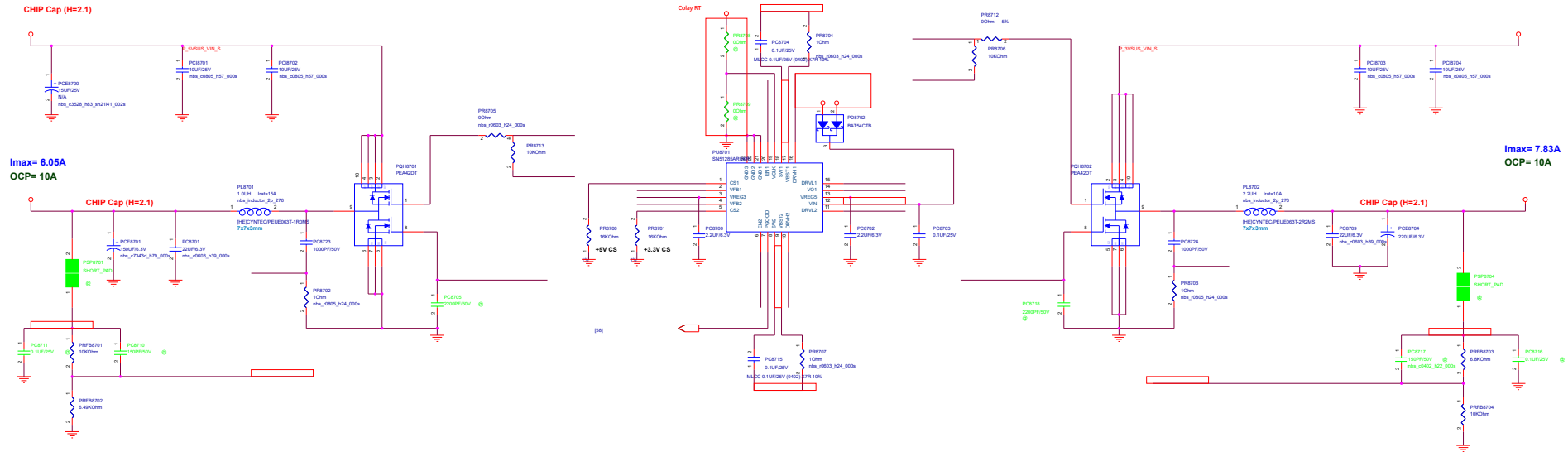
PT8S01



<Variant Name>		Project Name		Rev	
		GU603E		R1.0	
Title : PW_+1.8VSUS					
Size	Dept.:	NB Power team	Engineer:	Hon	
A3					
Date: Wednesday, January 18, 2023			Sheet	85	of 102

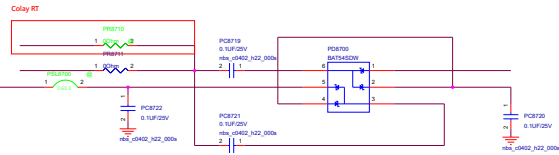
DDR Type	Vout	PU8601	PRFB8601	PRFB8602	PC8604	PR8604	PIN14 NET Name
DDR4	+1.2V	S1lery / SYV731RAC 06018-02990000	20K ohm 10G212200214030	19.6K ohm 10G2121196214010	2.2UF/6.3V 11G23222525360	@	+1.2V
LPDDR4x	+1.1V	S1lery / SYV731DRAC 06018-02990100	20K ohm 10G212200214030	23.2K ohm 10G212232214030	@	Dooh 10G212000004030	+1.1V
LPDDR5	+1.05V	S1lery / SYV731RAC 06018-02990000	20K ohm 10G212200214030	26.1K ohm 11G212261214010	2.2UF/6.3V 11G23222525360	@	+1.05V

+3VSUS / +5VSUS [System Power]



Imax= 6.05A
OCP= 10A

Imax= 7.83A
OCP= 10A



請 check 雙份線路 +12VSUS total 並聯對地電阻不得小於10kOhm



Adaptor Mode (MVP6)

	S0	S1	S2	S3	S4	S5	S6 with USB Charger
PS_ON	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1
3VSUS_ON	1	-	1	-	1	-	1
5VSUS_ON	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	1	-	1
BUSC_ECH	1	-	1	-	1	-	1
BUSB_ECH	1	-	1	-	1	-	1

Battery Mode (MVP6)

	S0	S1	S2	S3	S4	S5	S6 with USB Charger
PS_ON	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1
3VSUS_ON	1	-	1	-	1	-	1
5VSUS_ON	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	1	-	1
BUSC_ECH	1	-	1	-	1	-	1
BUSB_ECH	1	-	1	-	1	-	1

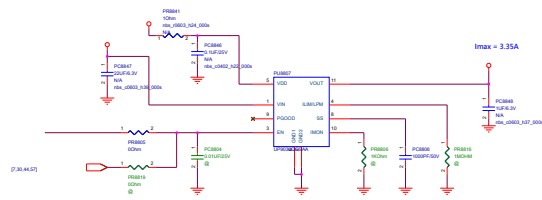
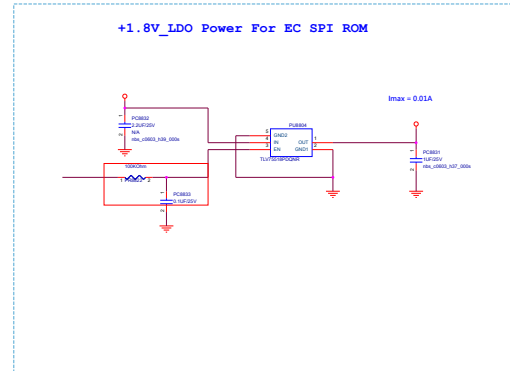
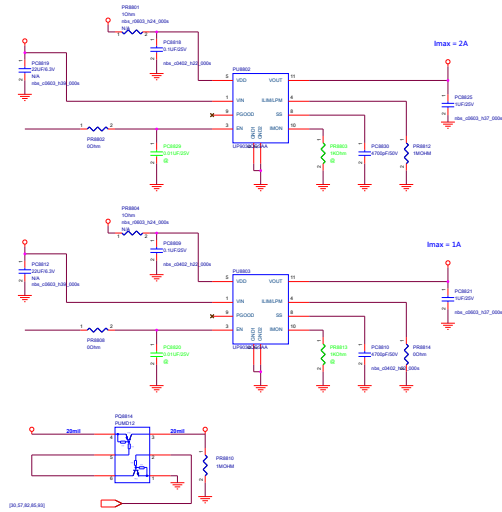
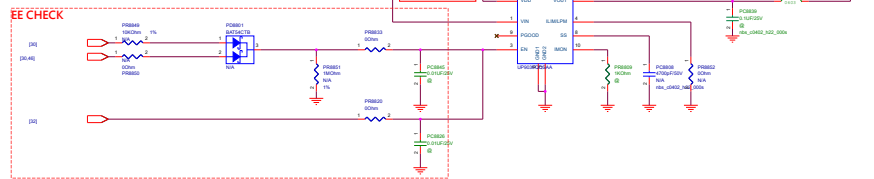
PT870* 請放置 PUS700旁,並請放置Trace上!

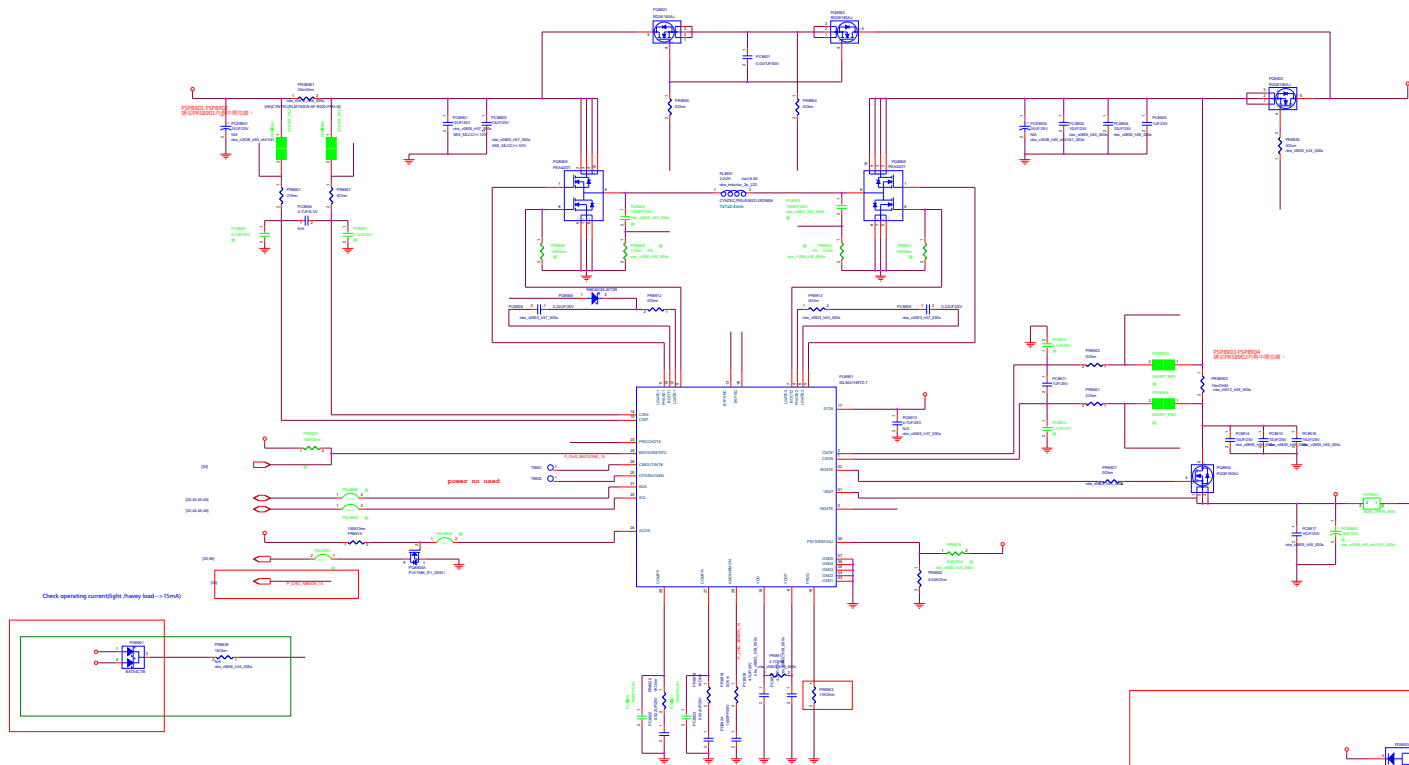


Standard Name

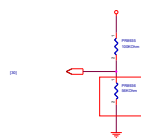
ASUS	Project Name	Rev.
GA502IV		B1.0
Title :	PW, +3VA, DSW, +5VSUS	
Dept. :	AS Power Team	Engineer: NREED3
Date :	Wednesday, January 16, 2025	Sheet 87 of 104

uP9030 LIM/LPM Setting 對應表		
LIM PIN	LPM (C30)	LIMIT Current
GND	Off	5A
5M to GND	Off	5A
Flow/VDD	On	5A



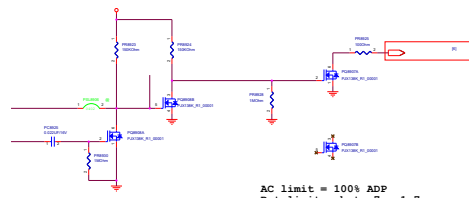


Adaptor select
total power = 90% ADP



Adaptor select				
	A. Reserve	B. Reserve		
PWRM01	10m	5m		
PWRM35				
0.4V	45W	120W		
0.8V	150W	150W		
1.2V	180W	180W		
1.6V	65W	230W		
2.0V	NA	280W		
2.4V	90W	330W		
2.8V	120W	240W		

HW_Throttle



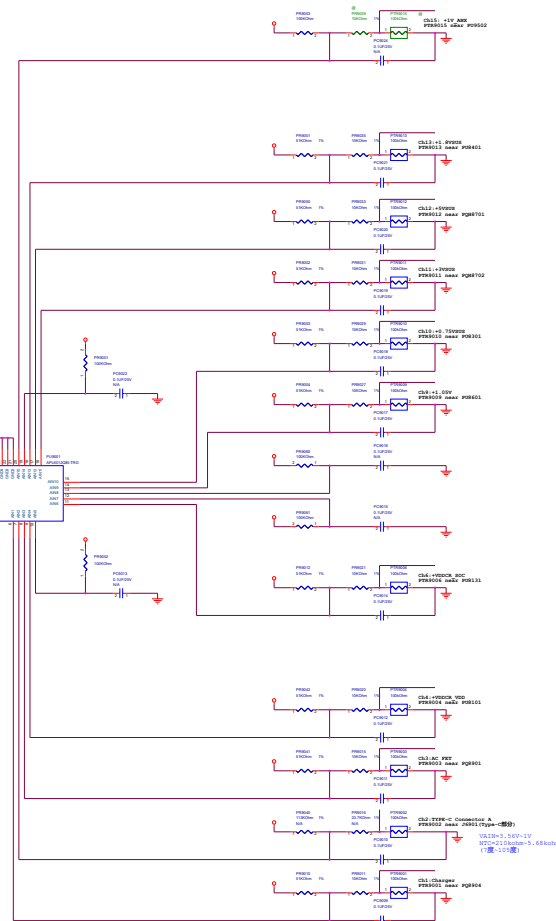
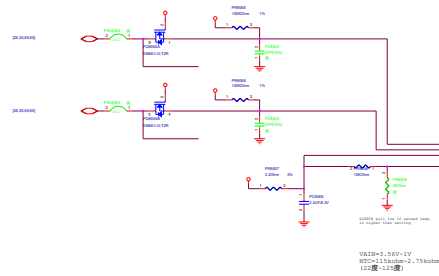
AC_LOSE_SOURCE_MB Side

P_AC_LOSS	CON_DET_TOWER	EC off/dischg	FRS_MOS
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

P90_PROTECTION

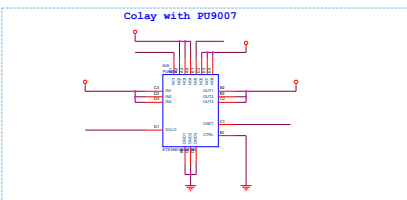
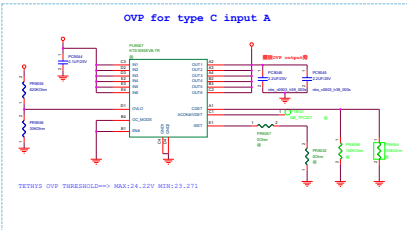
Address	0x70	0x71	0x72	0x73	0x74	0x75	0x76	0x77
0x0011	1.0x	1.5x	2x	3.0x	3.5x	4.0x	5.0x	6x
0x0012	Open	8.2x	6.2x	4.8x	4.7x	4.6x	2.7x	2x

Register Address							
Address	bit15	bit14	bit13	bit12	bit11	bit10	bit9
0/0	0	0	0	0	0	0	0
Function	Temp. alert threshold setting			Forward temp. data			bit9 = 0 bit8 = 0 bit7 = 0 bit6 = 0 bit5 = 0 bit4 = 0 bit3 = 0 bit2 = 0 bit1 = 0 bit0 = 0

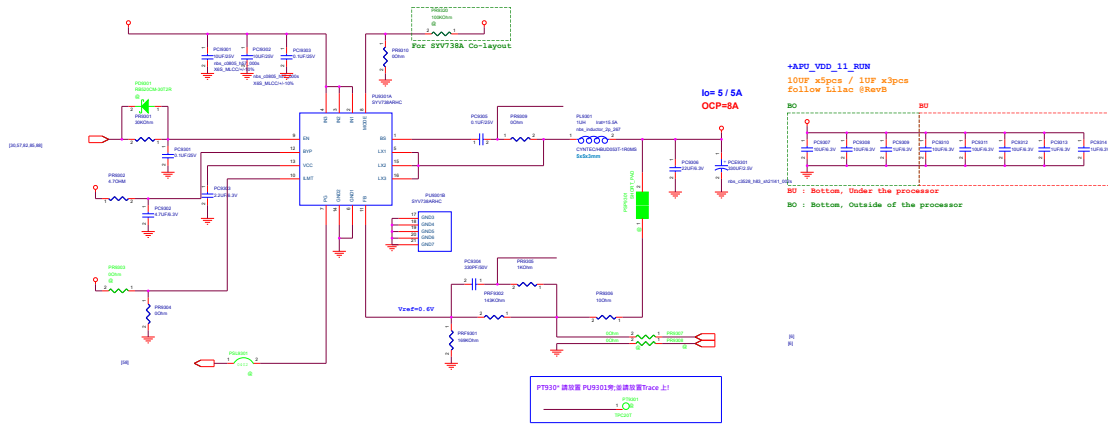


WIC	QWL	TGL
CE14	P0 in port B	P0 in port B
CE14	Slave Charger	Slave Charger
CE13	1.8VSS05	1.8VSS05
CE12	5VSS05	5VSS05
CE11	VXA_DSM	VXA_DSM
CE10	1.05VSS05	PEX_VDD
CE09	1.2V	1.2V
CE08	FBVSSQ	FBVSSQ
CE07	BVVDD	BVVDD
CE06	Vaa	AUX_PCH
CE05	VST	AUX_CPU
CE04	VCORE	VCORE
CE03	AC_FET	AC_FET
CE02	P0 in port A	P0 in port A
CE01	Charger Mos	Charger Mos

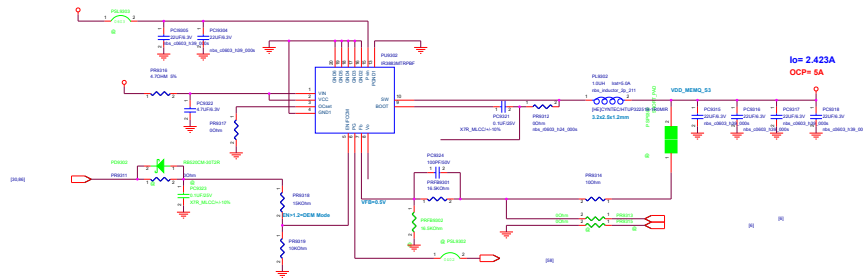
RTC	AND
CH15	SD in port B
CH14	Slave Charger
CH13	1.8VVSUS
CH12	5VSUS
CH11	3WA_DSW
CH10	0.75VSUS
CH09	1.2V
CH08	FBVDDQ
CH07	WVDDQ
CH06	VDDCR_SOC
CH05	PEX_VDD
CH04	VDDCR_VDD
CH03	AC FET
CH02	SD in port A
CH01	Charger Mos



+1.1VS [For APU]



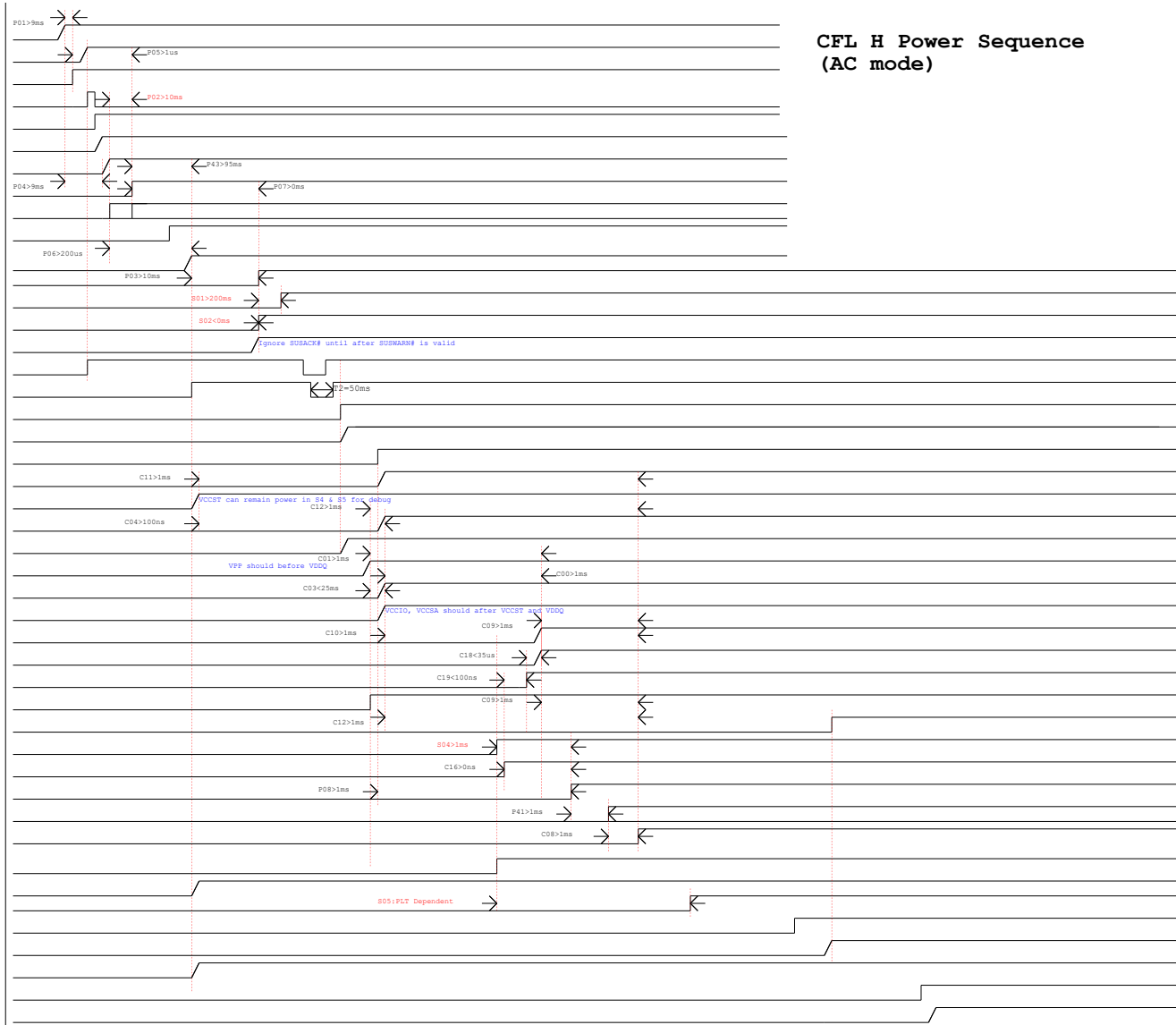
+0.5V [For APU]




```

C:CPU                                     (+RTCBAT)+3VA_RTC
P:PCH                                     (AC_BAT_SYS)+3VA/+5VA
S:PLT                                     (+3VA_RTC) RTCRST# (PCH)
Power                                     (Power)AC_IN_OC# (EC)
Signal                                     (EC) PS_ON(+3VA_EC)
                                           (PS_ON)+3VA_EC (EC)
                                           (3VADSW_ON)+3VA_DSW (3VA_DSW_PWRGD)
                                           (EC) DPWROK_EC (PCH)
                                           (+3VA_DSW) PM_BATLOW# (PCH)
                                           (PCH) PM_SLP_SUS# (EC)
(VSUS_ON)+1.0VSUS_VCCPRIM(1.0VSUS_PWRGD)
                                           (EC) PM_RSMRST#_PCH (PCH)
                                           (PCH) SUSWARN# (EC)
                                           (EC) ME_AC_PRESENT_PCH (PCH)
                                           (EC) PCH_SUSACK# (PCH)
                                           (PWR Switch) PWR_SW# (EC)
                                           (EC) PM_PWRBTTN# (PCH)
                                           (EC) SUSC_EC# (Power)
                                           (SUSC_EC#)+12V/+5V/+3V
                                           (EC) SUSB_EC# (Power)
                                           (SUSB_EC#)+12VS/+5VS/+3VS
                                           (SUSB_EC#)+1.0V_VCCST,VCCPLL
                                           (SUSB_EC#)+VCCIO,(+12VS)+VCCSTG
                                           (1.2V_ON)+2.5V(2.5V_PWRGD)
                                           (1.2V_ON)+VDDQ_CPU(1.2V_PWRGD)
                                           (+12VS)+VCCPLL_OC
                                           (SUSB_EC#)+VCCIO(VCCIO_PWRGD)
                                           (ALL_SYSTEM_PWRGD)+VCCSA(IMVP8_PWRGD)
                                           (DDR_VTT_CTRL)+0.6V
                                           (CPU) DDR_VTT_CTRL (Power)
                                           (Power)1.2V_PWRGD (AND)
                                           (Power) IMVP8_PWRGD
(AND)ALL_SYSTEM_PWRGD (CPU/PCH/EC/Power)
(ALL_SYSTEM_PWRGD) VCCST_PWRGD_CPU (CPU)
                                           (EC) PM_PWROK_PCH (PCH)
                                           (PCH) PLT_RST# (CPU/EC/Device)
                                           (PCH) H_CUPWRGD (CPU)
                                           (CPU) P_SVID_DATA_X2 (Power)
                                           (EC) PM_SYSPWROK_PCH (PCH)
                                           (PCH) PLT_RST# (CPU/EC/Device)
                                           (P_IMVP8_DRVON)+VCCOCCO(IMVP8_PWRGD)
                                           (CPU) H_THERMTRIP# (PCH)
                                           (PCH) DDR4_DRAMRST# (Memory)
                                           +VCCIO

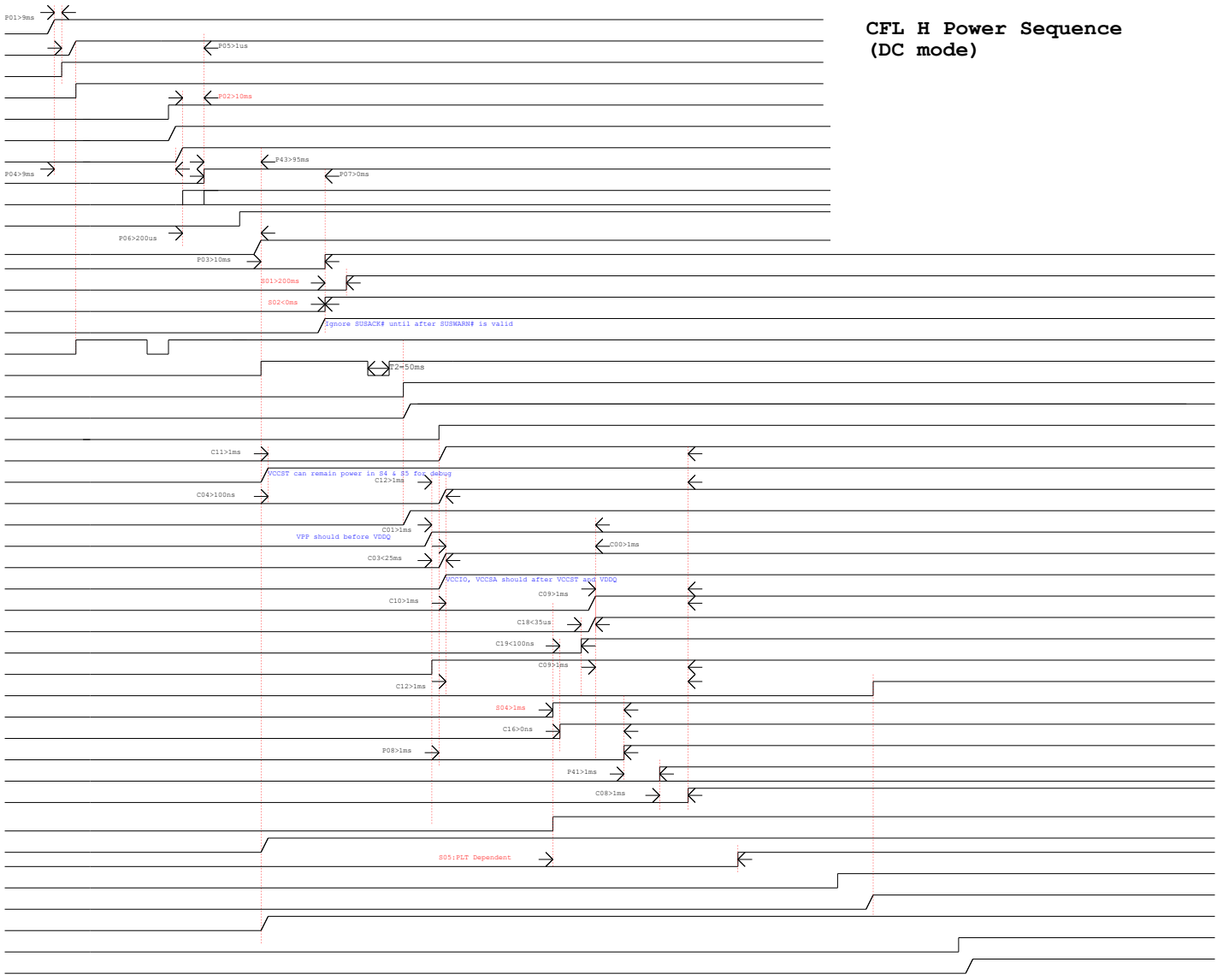
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CFL H Power Sequence
(AC mode)

DC-IN Mode

C:CPU (+RTCBAT)+3VA_RTC
P:PCH (AC_BAT_SYS)+3VA/+5VA
S:PLT (+3VA_RTC)RTCRST# (PCH)
Power (Power)AC_IN_OC# (EC)
Signal (EC)PS_ON (+3VA_EC)
(PS_ON)+3VA_EC (EC)
(3VADSW_ON)+3VA_DSW (3VA_DSW_PWRGD)
(EC)DPWROK_EC (PCH)
(+3VA_DSW)PM_BATLOW# (PCH)
(PCH)PM_SLP_SUS# (EC)
(VSUS_ON)+1.0VSUS_VCCPRIM (1.0VSUS_PWRGD)
(EC)PM_RSMRST#_PCH (PCH)
(PCH)SUSWARN# (EC)
(EC)ME_AC_PRESENT_PCH (PCH)
(EC)PCH_SUSACK# (PCH)
(PWR_Switch)PWR_SW# (EC)
(EC)PM_FWRBTN# (PCH)
(EC)SUSC_EC# (Power)
(SUSC_EC#)+12V/+5V/+3V
(EC)SUSB_EC# (Power)
(SUSB_EC#)+12VS/+5VS/+3VS
(VSUS_ON)+1.0V_VCCST,VCCPLL (VCCST_PWRGD)
(+VCCIO)+VCCSTG
(1.2V_ON)+2.5V (2.5V_PWRGD)
(1.2V_ON)+VDDQ_CPU (1.2V_PWRGD)
(+12VS)+VCCPLL_OC
(SUSB_EC#)+VCCIO (VCCIO_PWRGD)
(ALL_SYSTEM_PWRGD)+VCCSA (IMVP8_PWRGD)
(DDR_VTT_CTRL)+0.6V
(CPU)DDR_VTT_CTRL (Power)
(Power)1.2V_PWRGD (AND)
(Power)IMVP8_PWRGD
(AND)ALL_SYSTEM_PWRGD (CPU/PCH/EC/Power)
(ALL_SYSTEM_PWRGD)VCCST_PWRGD_CPU (CPU)
(EC)PM_PWROK_PCH (PCH)
(PCH)CLK_PCH_BCLK (CPU)
(PCH)H_CPUPWRGD (CPU)
(ALL_SYSTEM_PWRGD)P_IMVP8_EN_10 (Power)
(CPU)P_SVID_DATA_X2 (Power)
(EC)PM_SYSPWROK_PCH (PCH)
(PCH)PLT_RST# (CPU/EC/Device)
(P_IMVP8_DRVON)+VCCCORE (IMVP8_PWRGD)
(CPU)H_THERMTRIP# (PCH)
(PCH)DDR4_DRAMRST# (Memory)
+VCCGT



CFL H Power Sequence
(DC mode)

ASUS		Project Name	Rev
		GX502GX	1.0
Title : Power On Timing-DC mode			
Size	Dept.	ASUSTek COMPUTER INC.	Engineer: NR EE RD3
Date: Wednesday, January 18, 2023	Sheet	101	of 104

EE PART

GV301QH SKU Table

Part Number	PCB	SKU	CPU	L300B4X	VRAM	PD ID	
60NR06CO-MB621A	R2.0	GV301QH MB_32G/R9-5980HS//R2.0 (V4G)	R9-5980HS	32GB	V4G	WW	
60NR06CO-MB6110	R2.0	GV301QH MB_16G/R9-5980HS//R2.0 (V4G)	R9-5980HS	16GB	V4G	WW	
60NR06CO-MB6010	R2.0	GV301QH MB_8G/R9-5980HS//R2.0 (V4G)	R9-5980HS	32GB	V4G	WW	
60NR06CO-MB521A	R2.0	GV301QH MB_32G/R9-5900HS//R2.0 (V4G)	R9-5980HS	32GB	V4G	WW	
60NR06CO-MB511A	R2.0	GV301QH MB_16G/R9-5900HS//R2.0 (V4G)	R9-5980HS	32GB	V4G	WW	
60NR06CO-MB5010	R2.0	GV301QH MB_8G/R9-5900HS//R2.0 (V4G)	R9-5980HS	32GB	V4G	WW	
60NR06CO-MB423A	R2.0	GV301QH MB_32G/R7-5800HS//R2.0 (V4G)	R9-5980HS	32GB	V4G	WW	
60NR06CO-MB4110	R2.0	GV301QH MB_16G/R7-5800HS//R2.0 (V4G)	R9-5980HS	32GB	V4G	WW	
60NR06CO-MB401A	R2.0	GV301QH MB_8G/R7-5800HS//R2.0 (V4G)	R9-5980HS	32GB	V4G	WW	
60NR06CO-MB3210	R2.0	GV301QH MB_32G/R9-5980HS//R2.0 (V4G) (GE)	R9-5980HS	32GB	V4G	WW	
60NR06CO-MB3110	R2.0	GV301QH MB_16G/R9-5980HS//R2.0 (V4G) (GE)	R9-5980HS	32GB	V4G	WW	
60NR06CO-MB3010	R2.0	GV301QH MB_8G/R9-5980HS//R2.0 (V4G) (GE)	R9-5980HS	32GB	V4G	WW	
60NR06CO-MB2210	R2.0	GV301QH MB_32G/R9-5900HS//R2.0 (V4G) (GE)	R9-5980HS	32GB	V4G	WW	
60NR06CO-MB2110	R2.0	GV301QH MB_16G/R9-5900HS//R2.0 (V4G) (GE)	R9-5980HS	32GB	V4G	WW	
60NR06CO-MB2010	R2.0	GV301QH MB_8G/R9-5900HS//R2.0 (V4G) (GE)	R9-5980HS	32GB	V4G	WW	
60NR06CO-MB0210	R2.0	GV301QH MB_32G/R7-5800HS//R2.0 (V4G) (GE)	R9-5980HS	32GB	V4G	WW	
60NR06CO-MB0110	R2.0	GV301QH MB_16G/R7-5800HS//R2.0 (V4G) (GE)	R9-5980HS	32GB	V4G	WW	
60NR06CO-MB0010	R2.0	GV301QH MB_8G/R7-5800HS//R2.0 (V4G) (GE)	R9-5980HS	32GB	V4G	WW	

N-KEY

	White 128GB	128GB
R3104	#	10G212000044010
R3106	10G212000044010	#
R3107	#	10G212000044010
R3108	10G212000044010	#
R3164 R3174	#	10G212000044010
R3209 R3211	#	10G212100314010
Q3502 Q3505	#	07055-01803000

13. Audio Codec : 02043-00130000 (663-VA4)